SERVICE MANUAL FOR

8089P

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MiTAC

8089P N/B Maintenance

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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the brief introduction for MiTAC 8089P portable notebook computer system.

1.1.2 System Overview

The MiTAC 8089P model is designed for Intel Banias processor with 400MHz FSB with Micro-FCPGA package. It can support Banias 1.3GHz ~ 1.7GHz. ,Dothan 1.7GHz ~ 1.9GHz, and Banias Celeron 1.2GHz ~ 1.4GHz.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as AC Power indicator, Battery Power indicator, Battery status indicator, CD-ROM, HDD, NUM LOCK, CAP LOCK, and SCROLL LOCK. It also equipped with LAN, 56K Fax MODEM, 4 USB port, 3D stereo audio functions, S-Video and audio line out, and internal microphone.

The memory subsystem supports two expansion DDR SDRAM slot with unbuffered PC2100/PC2700 DDR-SDRAM

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The Montara-GME GMCH Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, Digital Video port (DVOB & DVOC) interface, and Intel Hub interface Technology connecting with Intel 82801DBM ICH4-M.

The Intel ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller with AC97 interface, the Ethernet includes a 32-bit PCI controller , the IDE Master/Slave controllers, and Intel Hub interface technology.

The VIA VT6105LOM “Rhine III” Ethernet controller is a cutting edge, feature-rich, and cost-competitive single ASIC chip solution for PC “LAN On Motherboard” applications or Low Cost NIC applications. The 6105LOM eases server processor utilization by optimizing throughput between NIC and PCI bus allowing data transfers of up to at 200Mbps in full duplex mode, without using the system CPU. The VT6105LOM contains advanced power management feature for low power consumption including Wake On LAN (WOL) and is implemented using a low power 0.22 micron design.

The TIE PCI1410A device is a high-performance PCI-to-PC Card controller that supports a single PC Card socket compliant with the PC Card Standard. The PCI1410A device provides features that make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The PC Card Standard retains the 16-bit PC Card specification defined in PCI Local Bus Specification and defines the new 32-bit PC Card, CardBus, as being capable of full 32-bit data transfers at 33 MHz. The PCI1410A device supports both 16-bit and CardBus PC Cards, powered at 5 V or 3.3 V, as required.

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The ALC101 is an 18-bit, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC101 AC'97 CODEC supports multiple CODEC extensions with independent variable sampling rates and built-in 3D effects. The ALC101 CODEC provides a pair of stereo outputs with independent volume controls and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC101 CODEC operates from a 5V/3.3V power supply with EAPD (External Amplifier Power Down) control for use in notebook and PC applications. The ALC101 integrates a 50mW/20ohm headset audio amplifier into the CODEC, saving BOM costs.

The CH7011A is a display controller device which accepts a digital graphics input signal, and encodes and transmits data to a TV output (analog composite, s-video or RGB). The device accepts data over one 12-bit wide variable voltage data port which supports five different data format including RGB and YcrCb. The TV-Out processor will perform non-interlace to interlace conversion with scaling and flicker filters, and encode the data into any of the NTSC or PAL video standards. The scaling and flicker filter is adaptive and programmable to enable superior text display. Eight graphics resolutions are supported up to 1024 X 768 with full vertical and horizontal underscan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for Macrovision and RGB bypass mode which enable driving a VGA CRT with the input data.

The Winbond mobile keyboard and embedded controller W83L950D architecture consists of a Turbo-51 core logic controller and surrounded by various components, 2K+256 bytes of RAM, 40K on-chip MTP-ROM, ISA or LPChost interface, 9 general purpose I/O port with 13 external interrupt source, 4 timers, 2 serial port, 2 SMBus interface for master and slave, 3 PS2 port, two 8-bits and two 16-bits PWM channels, 2 D-A and 8 A-D converters.

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A full set of software drivers and utilities are available to allow advanced operating systems such as Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

System Parts

- **CPU** : Intel Banias processor in Micro-FCPGA package
- **Synthesizer** : PLL207-151
- **North Bridge** : Montara-GME GMCH
- **South Bridge** : ICH4-M
- **TV-Out** : CH7011A
- **Keyboard System**: Winbond W83L950D Universal Controller
- **Fax/Modem** : Billonton MDC56S-I56Kbps Fax Modem
- **LAN Single Chip** : VT6105LOM
- **PCMCIA Controller** : TIPC1410A

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- **AC'97 Codec** : ALC101
- **Thermal Sensor** : ADT7460
- **System Flash Memory (BIOS)**

1.1.2.1 CPU Module : Banias

- Intel Banias Processors with 478 pins Micro-FCPGA package.
- The first Intel mobile processor with the Intel NetBurst micro-architecture which features include hyper-pipelined technology, a rapid execution engine, a 400MHz system, an execution trace cache, advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2).
- The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.
- Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.
- Support Enhanced Intel SpeedStep technology, which enables real-time dynamic switching of the voltageand frequency between two performance modes.

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1.1.2.2 Synthesizer : PLL207-151

- System frequency synthesizer: PLL207-151
- Programmable output frequency, divider ratios, output rise/fall time, output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watchdog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Use external 14.318MHz crystal.

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1.1.2.3 Montara-GME GMCH IGUI 3D Graphic DDR/SDR Chipset

Montara-GME GMCH IGUI Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, an AGP 4X interface, and Intel® I/O Hub architecture INTEL 82801DBM ICH4-M.

Montara-GME GMCH Host Interface features the AGTL & AGTL+ compliant bus driver technology with integrated on-die termination to support Intel Banias processors. Montara-GME GMCH provides a 12-deep In-Order-Queue to support maximum outstanding transactions up to 12. It integrated a high performance 2D/3D Graphic Engine, Video Accelerator and Advanced Hardware Acceleration MPEGI/MPEGII Video Decoder for the Intel Banias series based PC systems. It also integrates a high performance DDR333 Memory controller to

sustain the bandwidth demand from the integrated GUI or external AGP master, host processor, as well as the multi I/O masters. In addition to integrated GUI, Montara-GME GMCH also can support external AGP slot with AGP 1X/2X/4X capability and Fast Write Transactions. A high bandwidth and mature Intel®' I/O Hub architecture is incorporated to connect Montara-GME GMCH and INTEL 82801DBM ICH4-Mtogether. Intel®' I/O Hub architecture is developed into three layers, the Multi-threaded I/O Link Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Link layer, the Multi-threaded I/O Link Encoder/Decoder in INTEL 82801DBM ICH4-M to transfer dataw/533MB/s bandwidth from/to Multi-threaded I/O Link layer to/from Montara-GME GMCH, and the Multi-threaded I/O Link Encoder/Decoder in Montara-GME GMCH to transfer data w/533MB/s from/to Multi-threaded I/O Link layer to/from INTEL 82801DBM ICH4-M.

An Unified Memory Controller supporting DDR333 DRAM is incorporated, delivering a high performance data transfer to/from memory subsystem from/to the Host processor, the integrated graphic engine or external AGP master, or the I/O bus masters. The memory controller also supports the Suspend to RAM function by retaining the CKE# pins asserted in ACPI S3 state in which only AUX source deliver power. The Montara-GME GMCH adopts the Shared Memory Architecture, eliminating the need and thus the cost of the frame buffer memory by organizing the frame buffer in the system memory. The frame buffer size can be allocated from 8MB to 64MB.

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Features :

- Processor/Host Bus Support
  - Intel® Banias processor
  - 2X Address, 4X Data

- Support host bus Dynamic Bus Inversion (DBI)
- Supports system bus at 400MT/s (100 MHz)
- Supports 64-bit host bus addressing
- 8-deep In-Order-Queue
- AGTL+ bus driver technology with integrated GTL termination resistors and low voltage operation (1.05V)
- Supports Enhanced Intel® SpeedStep™ Technology (EIST) and Geyserville III
- Support for DPWR# signal to Banias processor for PSB power management

❖ **Memory System**

- Directly supports one DDR channel, 64-bits wide (72-b with ECC)
- Supports up 2 Double-Sided SO-DIMMs(4 rows populated) with unbuffered PC1600/PC2100/PC2700 DDR (with or without ECC)
- Supports 128-Mb, 256-Mb and 512-Mbit technologies providing maximum capacity of 1-GB with only x 16 devices
- All supported devices have 4 banks
- Supports up to 16 simultaneous open pages
- Supports page sizes of 2KB, 4KB, 8KB, and 16KB. Page size is individually selected for every row

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- Support for memory self refresh in C3
- UMA support only

❖ System Interrupt

- Supports 8259 and Processor System Bus interrupt delivery mechanism
- Supports interrupts signaled as upstream Memory Writes from PCI and Hub interface
- MSI sent to the CPU through the system Bus
- From IOxAPIC in ICH4-M
- Provides redirection for upstream interrupts to the System Bus
- Video Stream Decoder
- Improved HW Motion Compensation for MPEG2
- All format decoder (18 ATSC formats) supported
- Dynamic Bob and Weave support for Video Streams
- Software DVD at 60 fields/second and 30 frames/second full screen
- Support for 720x480 pixel resolution DVD quality encoding at low CPU utilization
- Video Overlay
- Single high quality scalable overlay and second Sprite to support second overlay

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- Multiple overlay functionality provided viaArithmetic Stretch Blt
- Direct YUV from Overlay to TV-out
- Independent Gamma Correction
- Independent Brightness / Contrast / Saturation
- Independent Tint / Hue support
- Destination Color keying
- Source Chromakeying
- Maximum source resolution of 1920x1080 pixels
- Maximum overlay clock of 133 MHz/200 MHz provides a pixel resolution up to 1600x1200@ 60Hz or 1280x1024@ 85 Hz

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❖ **Display**

- Analog Display Support
- 350 MHz integrated 24-bit RAMDAC that can drive a standard progressive scan analog monitor up to 1800x1350 @ 85 Hz
- Accompanying I2C and DDC channels provided through multiplexed interface Hotplug and display support
- Dual independent pipe with single display support Simultaneous: Same images and native display timings

on each display device

- Dedicated LFP (local flat panel) interface
  - Single l LVDS panel support up to SXGA+ panel resolution with frequency range from 25MHz to 112MHz per channel
  - Supports data format of 24 bpp
  - LCD panel power sequencing compliant with SPWG timing specification
  - Compliant with ANSI/TIA/EIA –644-1995 spec
  - Integrated PWM interface for LCD backlight inverter control
  - Bi-linear Panel fitting
- Tri-view support through LFP interface, TV ports and CRT
- Internal Graphics Features
- Core Frequency
  - Display Core frequency of 133MHz,200MHz,250MHz
  - Render Core frequency of 100 MHz, 133 MHz, 166 MHz, 200 MHz, 250 MHz
  - Intel® Dual-Frequency Graphics Technology
- 2D Graphics Engine
- Optimized 128 bit BLT engine
- Ten programmable and predefined monochrome patterns

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- Alpha Stretch Blt (via 3D pipeline)
- Anti-aliased lines
- Hardware-based BLT Clipping & Scissoring
- 32-bit Alpha Blended cursor
- Programmable 64*64 3-color Transparent cursor
- Color Space Conversion
- 3 Operand Raster BLTs
- 8-bit, 16-bit, and 32-bit color
- ROP support
- DIB translation and Linear/Title addressing
- 3D Graphics Engine
- 3D Setup and Render Engine
- Viewpoint Transform and Perspective Divide
- Triangle Lists, Strips and Fans support
- Indexed Vertex and Flexible Vertex formats
- Pixel accurate Fast Scissoring and Clipping operation
- Backface Culling support

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- DirectX™ and OGL Pixelization rules
- Enhanced Hardware Binning Instruction Set supported
- Bi-Cubic Filtering supported
- Linear Gamma Blending for Video Mixer Rendering (VMR)
- Video Mixer Rendering (VMR) supported
- Anti-Aliased Lines support
- Sprite Points support
- Zone Rendering
- Provides the highest sustained fill rate performance in 32-bit color and 24-bit W mode
- High quality performance Texture Engine
- 266 Mega Texel/speak performance
- Per Pixel Perspective corrected Texture Mapping
- Single Pass Texture Compositing (Multi-Texture) at rate
- Enhanced Texture Blending functions
- Twelve Level of Detail MIP Map Sizes from 1x1 to 2Kx2K
- Numerous Texture formats including 32-bit RGBA
- Alpha and Luminance Maps

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- Texture Chromakeying
- Bilinear, Trilinear, Anisotropic MIP-Mapped Filtering
- Cubic Environment Reflection Mapping
- Embossed Bump-mapping
- DXTn Texture Decompression
- 3D Graphics Rasterrization enhancements
- One Pixel per Clock
- Flat and Gouraud Shading
- Color Alpha Blending for Transparency
- Vertex and Programmable Pixel Fog and Atmospheric effects
- Color Specular Lighting
- Vertex and Programmable Pixel Fog and Atmospheric effects
- Z Bais support
- Dithering
- Line and Full-Scence Anti-Aliasing
- 16 and 24-bit Z Buffering
- 16 and 24-bit W Buffering

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- 8-bit Stencil Buffering
- Double and Triple Render Buffer support
- 16 and 32 –bit color
- Destination Alpha
- Vertex Cahec
- Maximum 3D resolution of 1600x1200 x32 bpp at 85 Hz
- Optimal 3D resolution supported
- Fast Clear support
- ROP support

❖ **HUB Interface for ICH4**

- 533 MB/s point to point hub interface to ICH4-M
- 66-M Hz base clock
- Supports the following traffic types to the ICH4-M
- Hub interface-to DRAM
- CPU-to-Hub interface
- Messaging

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- MSI interrupt messages
- Power Management state change
- SMI, SCI, and SERR error indication
- Power Management
  - SMRAM space remapping to A0000h (128-KB)
  - Supports extended SMRAM space above 256- MB ,additional 1 MB TSEG from top of Memory, cacheable (cacheability controlled by CPU)
  - APM rev 1.2 compliant power management
  - Supports Suspend to System Memory(S3),Suspend to Disk(S4) and Hard Off/Total Reboot(S5)
  - ACPI 1.0b,2.0 Support

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1.1.2.4 I/O Controller Hub : Intel 82801DBM

The Intel 82801DBM ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers, the Audio Controller with AC 97 Interface, the IDE Master/Slave controllers, and Intel® I/O Hub architecture. The PCI to LPC Bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O and legacy power management functionalities are integrated as well.

The integrated Universal Serial Bus Host Controllers features Dual Independent UHCI Compliant Host controllers with six USB ports delivering 480 Mb/s bandwidth and rich connectivity. Besides, Legacy USB devices as well as over current detection are also implemented.

The Integrated AC ’ 97 v2.3 compliance Audio Controller that features a 7-channels of audio speaker out and HSP v.90 modem support. Additionally, the AC97 interface supports 4 separate SDATAIN pins that is capable of supporting multiple audio codecs with one separate modem codec.

The integrated IDE Master/Slave controllers features Dual Independent IDE channels supporting PIO mode transfers up to 16 Mbytes/sec and Ultra DMA 33/66/100. It provides two separate data paths for the dual IDE channels that sustain the high data transfer rate in the multitasking environment.

Intel 82801DBM ICH4-M supports 6 PCI masters and complies with PCI 2.2 specification. It also incorporates the legacy system I/O like: two 82C37 compatible DMA controllers, Channels 0-3 are hardwired to 8 bit, three 8254 compatible programmable 16-bit counters channels 5-7, hardwired keyboard controller and PS2 mouse interface(not use in MiTAC 8089P model), Real Time clock with 512Bytes CMOS SRAM and two 82C59 compatible Interrupt controllers. Besides, the I/O APIC managing up to 14 interrupts with both Serial and FSB interrupt delivery modes is supported.

The integrated power management module incorporates the ACPI 1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec. v1.1. Numerous power-up events and power down events are also supported. 21 general purposed I/O pins are provided to give an easy to use logic for specific application. In addition, the Intel 82801DBM ICH4-M supports Deeper Sleep power state for Intel Mobile processor.

A high bandwidth and mature Intel®’ I/O Hub architecture is incorporated to connect Montara and Intel 82801DBM ICH4-M Hub interface together. Intel® I/O Hub architecture is developed.

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Features :

- PCI Bus Interface
- Supports PCI Revision 2.2 Specification at 33 MHz
- 133 MB/sec maximum throughput
- Supports up to six master devices on PCI
- One PCI REQ/GNT pair can be given higher arbitration priority (intended for external 1394 host controller)
- Support for 44-bit addressing on PCI using DAC protocol Integrated LAN Controller
- WFM 2.0 and IEEE 802.3 compliant
- LAN Connect Interface (LCI)
- 10/100 Mbit/sec Ethernet support Integrated IDE Controller
- Supports “Native Mode” register and interrupts
- Independent timing of up to 4 drives, with separate primary and secondary IDE cable connections
- Ultra ATA/100/66/33, BMIDE and PIO modes
- Tri-state modes to enable swap bay
- USB
- Includes three UHCI host controllers that support six external ports
- New: Includes one EHCI high-speed USB 2.0 Host Controller that supports all six ports

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- New: Supports a USB 2.0 high-speed debug port
- Supports wake-up from sleeping states S1–S5
- Supports legacy keyboard/mouse software AC-Link for Audio and Telephony CODECs
- Supports AC ’97 2.3
- New: Third AC_SDATA_IN line for three codec support
- New: Independent bus master logic for seven channels (PCM In/Out, Mic 1 input, Mic 2 input, modem in/out, S/PDIF out)
- Separate independent PCI functions for audio and modem
- Support for up to six channels of PCM audio output (full AC3 decode)
- Supports wake-up events Interrupt Controller
- Support up to eight PCI interrupt pins
- Supports PCI 2.2 message signaled interrupts
- Two cascaded 82C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts
- Supports serial interrupt protocol
- Supports processor system bus interrupt delivery New: 1.5 V operation with 3.3 V I/O
- 5 V tolerant buffers on IDE, PCI, USB over current and legacy signals Timers Based on 82C54

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- System timer, refresh request, speaker tone output Power Management Logic
- ACPI 2.0 compliant
- ACPI-defined power states (C1–C2, S3–S5)
- Supports Desktop S1 state (like C2 state, only STPCLK# active)
- ACPI power management timer
- PCI PME# support
- SMI# generation
- All registers readable/restorable for proper resume from 0V suspend states External Glue Integration
- Integrated pull-up, pull-down and series termination resistors on IDE, processor interface
- Integrated Pull-down and Series resistors on USB Enhanced Hub Interface Buffers Improve Routing flexibility (Not available with all Memory Controller Hubs)

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1.1.2.5 TV Encoder : CH7011A

The CH7011 is a Display controller device which accepts a digital graphics input signal, and encodes and transmits data to a TV output (analog composite, s-video or RGB). The device accepts data over one 12-bit wide variable voltage data port which supports five different data formats including RGB and YCrCb.The TV-Out processor will perform non-interlace to interlace conversion with scaling and flicker filters, and encode the data into any of the NTSC or PAL video standards. The scaling and flicker filter is adaptive and programmable to

enable superior text display. Eight graphics resolutions are supported up to 1024 by 768 with full vertical and horizontal underscan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for Macrovision™ and RGB bypass mode which enables driving a VGA CRT with the input data.

Features :

- Macrovision™ 7.X copy protection support
- TV output supporting up to 1024x768 graphics resolutions
- Programmable digital interface supports RGB and YCrCb
- True scale rendering engine supports underscan in all TV output resolutions
- Enhanced text sharpness and adaptive flicker removal with up to 7 lines of filtering
- Support for all NTSC and PAL formats
- Provides CVBS, S-Video and SCART (RGB) outputs
- TV connection detect
- Programmable power management
- 10-bit video DAC outputs
- Fully programmable through serial port
- Complete Windows and DOS driver support

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- Low voltage interface support to graphics device

1.1.2.6 KBC Controller_Winbond W83L950D

The Turbo-51 core logic of Winbond Keyboard controller is based on the industry standard 8032 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8032 instruction set.

The Winbond Keyboard controller separates the memory into two sections, the Program Memory and the Data Memory. The Program Memory, MTP-ROM, is used to store the instruction op-codes, and the Data Memory, RAM, is used to store data and now is consists of a 256 bytes scratch pad RAM and a 2K bytes external SRAM. The external SRAM can be accessed by either MOVX instruction in generally or to be a scratched ultra ROM for special purpose.

The brief descriptions of the internal blocks are shown as follows.

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Features :

- **Pin Out**
  - Pin–to-Pin compatible with Mitsubishi M3886 family (ISA mode)

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❖ Core Logic

- Turbo 8052 microprocessor based
- 256 bytes internal RAM
- 40K bytes embedded programmable flash memory
- 2K bytes external SRAM
- Host interface
- Software optional with ISA or LPC interface
- Primary programmable I/O address communication port in LPC mode
- Support either Parallel IRQ in ISA or SERIRQ in LPC interface
- Hardware Fast Gate A20 and KBRST support
- Port 92h support

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❖ SMBus

- Support 2 SMBus interface for master and slave

❖ Timers

- Support 4 Timer signal with 3 pre-scalars

- Timer 1 and 2 shard the same pre-scalar and are free-running only
- Timer X and Y have individual pre-scalar and support up to 4 control modes, free running, pulse output, event counter and pulse width measurement

❖ PWM

- Support 4 PWM channels

❖ ADC

- Support 2 DA output and 8 AD input
- DA 0, 1 are 8bits resolution
- AD 0-7 are firmware programmable optional with 10 or 8 bits resolution

❖ PS2

- Support 3 hardware PS2 channels
- Optional PS2 clock inhibit by hardware or firmware

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❖ **GPIO**

- Support 72 GPIO pins totally, and all are bit–addressable to facility firmware coding

❖ **FLASH**

- Support External On-Board Flash via Matrix interface (GP0, 1, 3)

❖ **ACPI**

- Support ACPI appliance
- Secondary programmable I/O address communication port in LPC mode

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1.1.2.7 Fast Ethernet Controller VT6105LOM

The VIA Rhine III VT6105LOM is a 10/100Mbps Fast Ethernet controller designed to provide system designers an easy to integrate single chip solution, with advanced management and power conservation features. Featuring a 3-in-1 design the VIA VT6105LOM integrates the physical, media, and management layers into a single chip.

Features :

❖ Single chip full/half duplex 10/100Mbps Fast Ethernet Management Controller

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- IEEE 802.3/802.3u 10BASE-T and 100BASE-T Compatible
- 32bit PCI Bus-Master Interface
- VIA Rhine based CSR definition provides efficiency PCI bus-mastering
- Low power 100base-TX transceiver embedded Support 10Mbps and 100Mbps N-way Auto-negotiation operation Support Auto-MDIX function
- Enhancement MAC functions for 802.3 networking 802.1 Priority Transmit Maximum eight priority queues by drivers programmable 802.1q Multiple VLAN support VLAN long frames support (1518+4bytes) VLAN tag auto inserting and extracting on TX and RX side (VT6105LOM) NIC auto filtering on VLAN ID optional (VT6105LOM)
- IP header Checksum Offload supporting for Ipv4 frames. Support both of TCP and UDP protocol (VT6105LOM)
- Support Physical, Broadcast, and Multicast addresses filtering using both hashing table look-up and perfect-matchmechanisms (VT6105LOM)
- 12 sets hardware 16 bit MIB counters (VT6105LOM)
- Fiber Optic network support (VT6105LOM)
- WFM 2.0 (VT6105LOM)
- DMI 2.0 (H/W)
- IO 3.3v with PCI bus 5V tolerant / Core 2.5v power, using low power 0.22um TSMC CMOS process, 128pin PQFP package.

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1.1.2.8 FAX/MODEM Module_MDC56S-1

- Made by Billionton Computer corporation
- Integrated PCI v2.2 Interface
- Host-based ITU V.70 DSVD.
- Operation support: Windows 95/NT/ME/2000
- K56flex for internet connection rates approaching 56kbits/s.
- Data Modes capabilities
  - Support 2 DA output and 8 AD input
  - DA 0, 1 are 8bits resolution
  - AD 0-7 are firmware programmable optional with 10 or 8 bits resolution.
- FAX mode capabilities:
  - ITU-T V.17, V.29, V.27ter, and V.21 CH 2
  - TIA/EIA 578 Class 1 FAX
- V.80 Host Controlled Communication Protocol Standards
  - H.324 Interface Support
- On Chip PnP Logic
- ACPI support “On Now”

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- Support “Call ID”
- PC 97 Compliant – Unimodem/V Compliant
- Low Power Consumption
- Operation Voltage 3.3V

1.1.2.9 PCMCIA Controller_ TI PCI1410A + TI TPS2211A

PCI1410A

The TIE PCI1410A device is a high-performance PCI-to-PC Card controller that supports a single PC Card socket compliant with the PC Card Standard. The PCI1410A device provides features that make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The PC Card Standard retains the 16-bit PC Card specification defined in PCI Local Bus Specification and defines the new 32-bit PC Card, CardBus, as being capable of full 32-bit data transfers at 33 MHz. The PCI1410A device supports both 16-bit and CardBus PC Cards, powered at 5 V or 3.3 V, as required.

The PCI1410A device is compliant with the PCI Local Bus Specification, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card DMA transfers or CardBus PC Card bridging transactions. The PCI1410A device also is compliant with the latest PCI Bus Power Management Interface Specification and PCI Bus Power Management Interface Specification for PCI to CardBus Bridges.

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All card signals are buffered internally to allow hot insertion and removal without external buffering. The PCI1410A device is register-compatible with the IntelE 82365SL-DF and 82365SL ExCA controllers. The PCI1410A internal data-path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The PCI1410A device also can be programmed to accept fast-posted writes to improve system-bus utilization.

Multiple system-interrupt signaling options are provided, including: parallel PCI, parallel ISA, serialized ISA, and serialized PCI. Furthermore, general-purpose inputs and outputs are provided for the board designer to implement sideband functions. Many other features designed into the PCI1410A device, such as socket-activity light-emitting diode (LED) outputs, are discussed in detail throughout the design specification.

An advanced complementary metal-oxide semiconductor (CMOS) process achieves low system power consumption, while operating at PCI clock rates up to 33 MHz. Several low-power modes enable the host power management system to further reduce power consumption.

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Features :

- Ability to wake from D3hot and D3cold
- Full compatibility with the Intel 430TX (Mobile Triton II) chipset
- A 144-terminal low-profile QFP (PGE), 144-terminal MicroStar BGAE ball grid array (GGU) package, or 209-terminal MicroStar BGAE (GHK) package
- 3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments

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- Mix-and-match 5-V/3.3-V 16-bit PC Cards and 3.3-V CardBus Cards
- Single PC Card or CardBus slot with hot insertion and removal
- Burst transfers to maximize data throughput on the PCI bus and the CardBus bus
- Parallel PCI interrupts, parallel ISA IRQ and parallel PCI interrupts, serial ISA IRQ with parallel PCI interrupts, and serial ISA IRQ and PCI interrupts
- Serial EEPROM interface for loading subsystem ID and subsystem vendor ID
- Pipelined architecture allows greater than 130 Mbit/s sustained throughput from CardBus to PCI and from PCI to CardBus
- Interface to parallel single-slot PC Card power-switch interfaces like the TIE TPS2211 device
- Up to five general-purpose I/Os
- Programmable output select for CLKRUN
- Five PCI memory windows and two I/O windows available to the 16-bit PC Card socket
- Two I/O windows and two memory windows available to the CardBus socket
- Exchangeable card architecture (ExCA) compatible registers are mapped in memory and I/O space
- Compatibility with Intel 82365SL-DF and 82365SL registers
- Distributed DMA (DDMA) and PC/PCI DMA
- 16-bit DMA on the PC Card socket
- Ring indicate, SUSPEND, PCI CLKRUN, and CardBus CCLKRUN

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- Socket-activity LED pins
- PCI bus lock (LOCK)
- Advanced submicron, low-power CMOS technology
- Internal ring oscillator

1.1.2.10 TPS2211A(Power Switch)

The TPS2211A PC Card power-interface switch provides an integrated power-management solution for a single PC Card. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit, using the Texas Instruments LinBiCMOS process. The circuit allows the distribution of 3.3-V, and/or 5-V card power, and is compatible with many PCMCIA controllers. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to the PC Card.

The TPS2211A features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5 V. Bias power can be derived from either the 3.3-V or 5-V inputs. This facilitates low-power system designs such as sleep mode and pager mode where only 3.3 V is available.

End equipment for the TPS2211A includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners.

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Features :

- Fully Integrated VCC and Vpp Switching for Single-Slot PC Card. Interface
- Low r_{DS}(on) (90-mΩ 5-V VCC Switch and 3.3-V VCC Switch)
- Compatible With Controllers From Cirrus, Ricoh, O2Micro, Intel, and Texas Instruments
- 3.3-V Low-Voltage Mode
- Meets PC Card Standards
- Short-Circuit and Thermal Protection
- Space-Saving 16-Pin SSOP (DB)
- Compatible with 3.3-V, and 5-V PC Cards
- Break-Before-Make Switching

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1.1.2.11 AC'97 Codec _ Realtek ALC101

The ALC101 is an 18-bit, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC101 AC'97 CODEC supports multiple CODEC extensions with independent variable sampling rates and built-in 3D effects. The ALC101 CODEC provides a pair of stereo outputs with independent volume controls and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC101 CODEC operates from a 5V/3.3V power supply with EAPD

(External Amplifier Power Down) control for use in notebook and PC applications. The ALC101 integrates a 50mW/20ohm headset audio amplifier into the CODEC, saving BOM costs. The ALC101 CODEC supports host/soft audio from Intel 810/815/820/845 chipsets as well as audio controller based VIA/SIS/ALI chipsets. Bundled Windows series drivers (Win95/98/ME/2000/XP/NT) and sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation, 5-band equalizer) provide an excellent entertainment package for PC users. Finally, internal PLL circuits generate required timing signals, eliminating the need for external clocking devices.

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Features :

- Single chip audio CODEC with high S/N ratio
- Compliant with AC'97 2.2 specification
- 16-bit stereo full-duplex CODEC with fixed 48KHz sampling rate
- 3 analog line-level stereo inputs with 5-bit volume control: LINE-IN, CD-IN, AUX-IN
- 1 analog line-level mono input: PHONE-IN
- 1 MIC input
- Power management
- 3D Stereo Enhancement
- LINE output with 50mW/20Ω headphone driver
- External amplifier power down capability

- Power supply: Digital: 3.3V Analog: 5V/3.3V
- Clocking by external 14.318MHz or 24.576MHz source to save crystal
- Standard 48-pin LQFP Package

1.1.2.12 Thermal Sensor_ ADM1021A

The ADT7460 dBCOOL™ controller is a systems monitor and multiple PWM fan controller for noise-sensitive applications requiring active system cooling. It can monitor the temperature of up to 2 remote sensor diodes, plus its own internal temperature. It can measure and control the speed of up to 4 fans so that they operate at the lowest possible speed for minimum acoustic noise. The Automatic Fan Speed Control Loop optimizes fan speed for a given temperature. A unique Dynamic TMIN Control Mode enables the system thermals/acoustics to be intelligently managed. The effectiveness of the System's Thermal Solution can be monitored using the THERM input. The ADT7460 also provides critical Thermal Protection to the system using the bidirectional THERM pin as an output to prevent system or component overheating.

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1.1.2.13 System Flash Memory (BIOS)

- 4M bit Flash memory
- Flashed by 5V only
- User can upgrade the system BIOS in the future just running flash program
- See Software BIOS Specification

1.2 Other Functions

1.2.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Reserve	
Fn + F2	Reserve	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	LCD/External CRT Switching	Rotate display mode in LCD only, CRT only and simultaneously display.
Fn + F6	Brightness Down	Decreases the LCD brightness
Fn + F7	Brightness Up	Increases the LCD brightness
Fn + F8	Reserve	
Fn + F9	Reserve	
Fn + F10	Battery beep enable/disable	Battery low beep sound enable/disable
Fn + F11	Panel Off/On	Toggle panel Off/On
Fn + F12	Suspend to DRAM/HDD	Force the computer into either Suspend to HDD or Suspend to RAM mode.

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1.2.2 Power On/Off/Suspend/Resume Button

1.2.2.1 APM Mode

At APM mode, power button is on/off system power.

1.2.2.2 ACPI Mode

At ACPI mode, power button behavior was set by windows power management control panel.

You could set “standby” , “power off” or “hibernate”(must enable hibernate function in power management) to power button function. Continue pushing power button over 4 seconds will force system off at ACPI mode.

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1.2.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off

4. Hibernate (must enable hibernate function in power management)

1.2.4 LED Indicators

System has eight status LED indicators to display system activity, which include three at front side and five above keyboard.

Three LED indicators on LCD panel:

From left to right that indicate: RF, POWER and BATTERY STATUS.

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1.2.5 Fan Power On/Off Management

FAN is controlled by W83L950D embedded controller using ADT7460 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster fan speed.

1.2.6 CMOS Battery

CR2032 3V 220mAh lithium battery.

When AC in or system main battery inside, CMOS battery will consume no power. AC or main battery not exist, CMOS battery life at less (220mAh/5.8uA) 4 years. Battery was put in battery holder, can be replaced.

1.2.7 I/O Port

- One Power Supply Jack
- One External CRT Connector For CRT Display
- One S-Video TV Output Connector
- Supports four USB2.0 port for all USB devices
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN
- Microphone Input Jack
- One CardBus Sockets for one type II PC card extension

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1.3 Peripheral Components

1.3.1 LCD Panel

- 1st Source: Hydis 15” TFT: HT15X34-100
- 2nd Source: AU 15” TFT : B150XG02
- Please reference the spec for detail.

1.3.2 Ext. Floppy Disk Drive

- External USB 3.5” 1.44MB /1.2 MB/720KB FDD (Option)
- 1st Source :Mitsumi D353FUE

1.3.3 HDD

- Fujitsu 30GB: MHT2030AT / 40GB: MHT2040AT/ 60GB : MHT2060AT
- HGST 30GB: IC25N030ATMR04-0 /40GB: IC25N040ATMR04-0 /60GB: IC25N060ATMR04-0 /80GB: IC25N080ATMR04-0

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1.3.4 CD ROM Drive

- 1st source : TEAC CD-224E-C93 (24X)

1.3.5 DVD ROM Drive

- 1st source : MKE :SR-8177-B (8X DVD-ROM/24X CD-ROM)

1.3.6 COMBO Drive

- 1st source : Liteon: LSC-24082K (24 X 24 X 8 X 24) (Read:8X DVD-ROM/24X CD-ROM ; Write :24X CD-R/24X CD-RW)
- 2nd source : QSI: SBW-242 (24X10X8X24) (Read:8X DVD-ROM/24X CD-ROM ; Write :24X CD-R/10X CD-RW)
- 3rd source : KME: UJDA750MT (24 X 24 X 8 X 24) (Read:8X DVD-ROM/24X CD-ROM ; Write :24X CD-R/24X CD-RW)

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1.3.7 Super COMBO Drive

- 1st source : MKE UJ810B (Read : 8X DVD-ROM/24X CD-ROM ; Write 16X CD-R / 4X CD-RW / 8X High Speed CD-RW / 2X DVD-R /1X DVD-RW / 2X DVD-RAM)

- 2nd source : QSI SDW-041 (DVD+RW)
- 3rd source: Liteon: SDW-421S
- 4th source: HLDS GWA-4040N (8X DVD-ROM / 24X CD-ROM)

1.3.8 Keyboard

- TJME 19mm pitch/3.0mm stroke

1.3.9 Track Pad : Synaptics TM41PUM311-2

- Accurate positioning
- Low fatigue pointing action
- Low profile
- No moving part, high reliability
- Low power consumption
- Environmentally sealed
- Compact size
- Software configurable

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- Low weight
- Operating temperature: 0 to 60 degree C
- Operating humidity : 5%-95% relative humidity, non condensing
- Storage temperature: -40 to +65 degree C
- ESD: 15KV applied to front surface SEE ESD Testing specification PN 520-000270-01
- Power supply voltage : 5.0Voltage ± 10%
- Power supply current : 4.0mA max operating

1.3.10 Fan

- HY45J05-001

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1.4 Power Management

The MiTAC 8089P system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.4.1 System Management Mode

1.4.1.1 Full On Mode

In this mode, each devices is running with the maximal speed. CPU clock is up to its maximum.

1.4.1.2 Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

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1.4.1.3 Standby Mode

For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

- CPU: Stop grant
- LCD: Backlight off
- HDD: Spin down

1.4.1.4 Suspend to DRAM and HDD

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

❖ **Suspend to DRAM**

- CPU: off
- NB: Partial off
- VGA: Suspend
- PCMCIA: Suspend
- Audio: off
- SDRAM: Self Refresh

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❖ **Suspend to HDD**

- All devices are stopped clock and power-down
- System status is saved in HDD
- All system status will be restored when powered on again

1.4.2 Other Power Management Functions

❖ HDD & Video Access

System has the ability to monitor video and hard disk activity. User can enable monitoring video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

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1.5 Appendix 1: Intel 82801DBM ICH4-M GPIO Definitions

Pin Name	MUX Function	GPIO Function	Power Plane
GPIO0	CRT_IN#	GPI	MAIN
GPIO1	X	GPI	MAIN
GPIO2	INT_PIRQE#	GPI	MAIN
GPIO3	INT_PIRQF#	GPI	MAIN
GPIO4	INT_PIRQG#	GPI	MAIN
GPIO5	X	GPI	MAIN
GPIO6	AGP_BUSY#	GPI	MAIN
GPIO7	KB_US/JP#	GPI	MAIN
GPIO8	EXTSMI#	GPI	RESUME
GPIO11	SMBALERT#	GPI	RESUME
GPIO12	SCI#	GPI	RESUME
GPIO13	WAKE_UP#	GPI	RESUME
GPIO16	SIDE_OFF#	GPO	MAIN
GPIO17	PIDE_OFF#	GPO	MAIN
GPIO18	STOP_PCI	GPO	MAIN
GPIO19	SUSA#	GPO	MAIN
GPIO20	STOP_CPU	GPO	MAIN
GPIO21	X	GPO	MAIN
GPIO22	CPUPERF#	OD	MAIN

Pin Name	MUX Function	GPIO Function	Power Plane
GPIO23	X	O	MAIN
GPIO24	PCLKRUN#	GPIO	RESUME
GPIO25	X	GPIO	RESUME
GPIO27	X	GPIO	RESUME
GPIO28	X	GPIO	RESUME
GPIO32	WIRELESS_PD#	GPIO	MAIN
GPIO33	LCDID0	GPIO	MAIN
GPIO34	LCDID1	GPIO	MAIN
GPIO35	LCDID2	GPIO	MAIN
GPIO36	SIDE_IN#	GPIO	MAIN
GPIO37	ICH_SIDE_IN#	GPIO	MAIN
GPIO38	IDERST#	GPIO	MAIN
GPIO39	MINIPCI_ACT#	GPIO	MAIN
GPIO40	DEBIG_EN	GPIO	MAIN
GPIO41	SIDEDET	GPIO	MAIN
GPIO42	SPK_OFF	GPIO	MAIN
GPIO43	SIDERST#	GPIO	MAIN

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1.6 Appendix 2: MiTAC 8089P Product Specification

Model	8089P System A	8089P System B
Core logic	Intel 855GME + ICH4M	Intel 855GME + ICH4M
CPU	Intel Pentium M 1.3G	Intel Pentium M 1.6G
Display	14” XGA Hydis :HT14X19-100	15” XGA Samsung: LTN150XB-L03
HDD	HGST 40GB IC25N040ATMR04-0	Fujitsu 40GB MHT2040AT
RAM Module	DDR 333 MHz 256MB DDR memory Module Apacer 77.10634.110 (Infineon 32x8)	DDR 333 MHz 512MB DDR memory Module Twinmos M2S5J08D1AMC5F1611A-T,TWINMOS
Modem	Billionton :MDC56S-I	Billionton :MDC56S-I
Video Controller	Intel 855 GME Int.	Intel 855 GME Int.
Audio	Audio Power Amplifier: TI /TPA0212 AC 97 CODEC: Realtek ALC101	Audio Power Amplifier: TI /TPA0212 AC 97 CODEC: Realtek ALC101
Wireless lan	Intel Pro/Wireless 2100	Intel Pro/Wireless 2100
PCMCIA	TI PCI1410A / Power Switch : TI TPS2211A	TI PCI1410A / Power Switch : TI TPS2211A
Keyboard Controller	Winbond W83L950D	Winbond W83L950D
LAN Controller	VIA VT6105LOM	VIA VT6105LOM
AC Adapter	60W(Delta)	60W(Delta)
Battery	6 cell 2000mAH (Panasonic)	9 cell 2000mAH (Panasonic)

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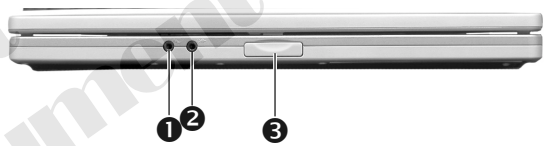
2. System Assembly & Disassembly

2.1 System View

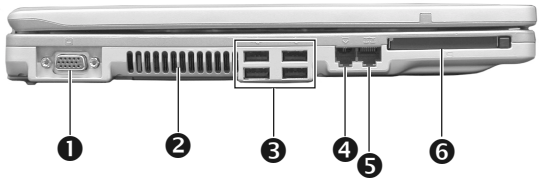
2.1.1 Front View

❶ External Microphone Input
❷ External Audio output
❸ Top Cover Latch



2.1.2 Left-Side View

❶ VGA Port
❷ Ventilation Openings
❸ USB Ports *4
❹ Phone Line Input
❺ LAN Connector
❻ PC Card Slot



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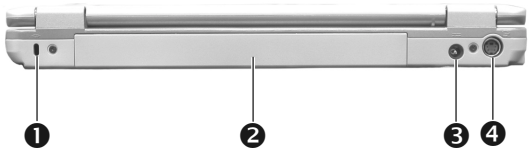
2.1.3 Right-Side View

❶ CD-ROM/DVD-ROM Drive

2.1.4 Rear View

❶ Lock hole
❷ Battery Pack
❸ Power Connector
❹ S-Video Port



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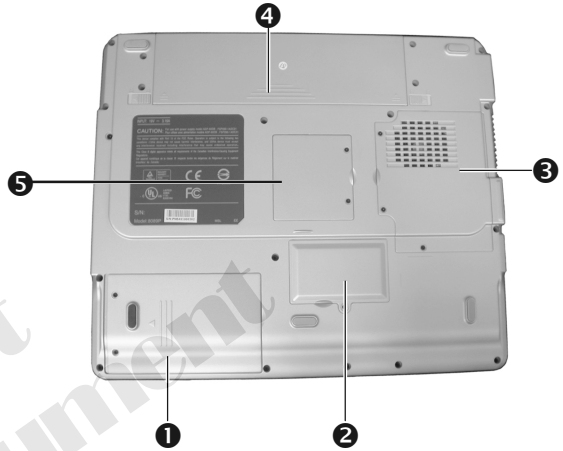
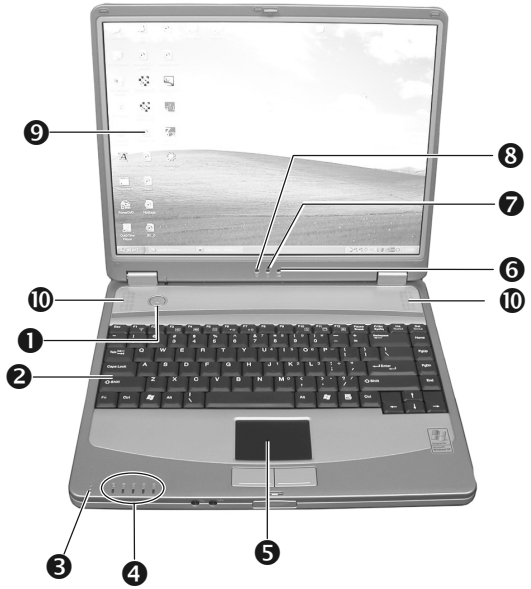
2.1.5 Bottom View

❶ Hard Disk Drive Cover
❷ DDR-SDRAM Cover
❸ CPU Cover
❹ Battery Pack
❺ Mini PCI Cover



2.1.6 Top-Open View

❶ Power Button
❷ Keyboard
❸ Internal Microphone
❹ Device LED Indicators
❺ Touch Pad
❻ Battery Power Indicator
❼ Battery Charge Indicator
❽ AC Power Indicator
❾ LCD Screen
❿ Stereo Speaker



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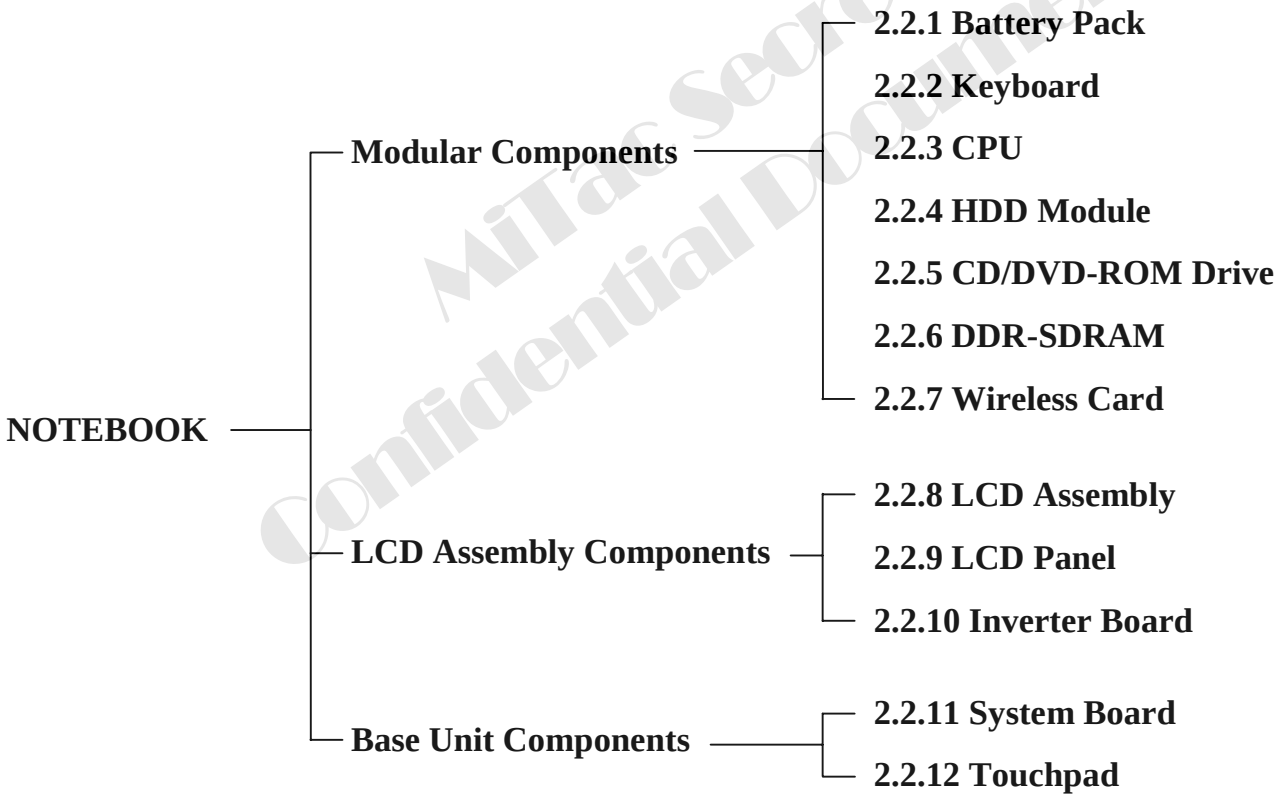
2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



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2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Pull the battery pack out of the compartment (❷) while sliding and holding the release lever outwards to the "unlock" ( ) position (❶). (Figure 2-1)

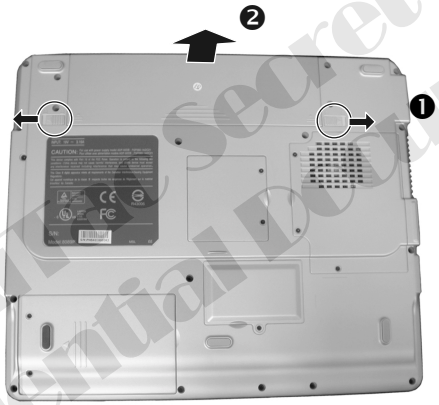

Figure 2-1 Remove the battery pack

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Reassembly

1. Push the battery pack into the compartment. The battery pack should be correctly connected when you hear a click-ing sound.
2. Slide the release lever to the "lock" ( ) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 disassembly)
2. You can push the keyboard cover to loose the locks from the battery compartment. (Figure 2-2)

Figure 2-2 Push the keyboard cover

Figure 2-3 Remove the keyboard cover

3. Lift the keyboard cover up. (Figure 2-3)

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4. Slightly lift up the keyboard. (Figure 2-4)

Figure 2-4 lift up the keyboard

Figure 2-5 Disconnect the cable

5. Then disconnect the cable from system board to detach the keyboard. (Figure 2-5)

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Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Fit the keyboard cover.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.3 CPU

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (Refer to section 2.2.1 disassembly)
2. Remove three screws fastening the CPU compartment cover. (Figure 2-6)

Figure 2-6 Remove the CPU compartment cover

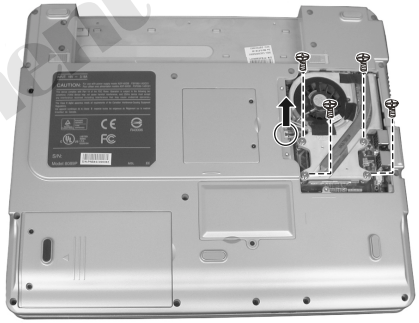

Figure 2-7 Remove the heatsink

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3. Remove four spring screws that secure the heatsink and disconnect the fan's power cord to detach the heatsink from the CPU compartment. (Figure 2-7)

4. Loosen the screw by a flat screwdriver,upraise the CPU socket to unlock the CPU. (Figure 2-8)

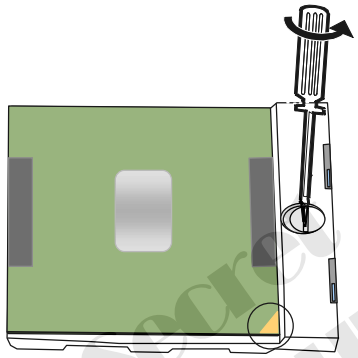

Figure 2-8 Remove the CPU socket

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Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with four spring screws.
3. Replace the heatsink compartment cover and secure with three screws.
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (Refer to section 2.2.1 disassembly)
2. Remove two screws fastening the HDD compartment cover, and lift the cover up. (Figure 2-9)

Figure 2-9 Remove the HDD cover

Figure 2-10 Remove the HDD drive

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3. Slide the hard disk drive leftwards to unplug the drive. (Figure 2-10)

4. Loosen the four screws to separate the hard disk drive from the bracket. (Figure 2-11)

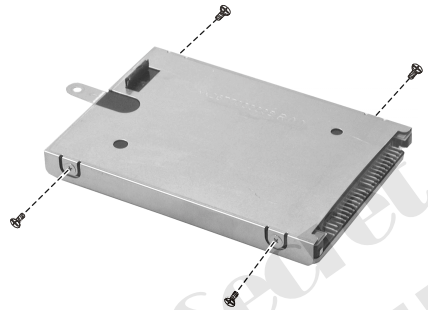

Figure 2-11 Free the HDD drive

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Reassembly

1. To install the hard disk drive, place it in the bracket and secure with four screws.
2. Put the hard disk drive in the compartment and slide it inwards to plug and secure with one screw.
3. Replace the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (Refer to section 2.2.1 disassembly)
2. Loosen the one screw that secure the CD/DVD-ROM drive. (Figure 2-12)

Figure 2-12 Remove the CD/DVD-ROM

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3. Put the notebook back to the upright position. Then insert a small rod, such as a straightened paper clip, into the drive's manual eject hole and push firmly to release the tray (❶). Pull the tray out until fully extended (❷), then carefully pull harder to remove the CD/DVD-ROM drive. (Figure 2-12)

Reassembly

1. To replace the CD/DVD-ROM drive, slide and push it all the way into the compartment to plug.
2. Secure the CD/DVD-ROM drive with one screw.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.6 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (Refer to section 2.2.1 disassembly)
2. Loosen one screw that secure the DDR compartment cover. (Figure 2-13)

Figure 2-13 Remove the cover

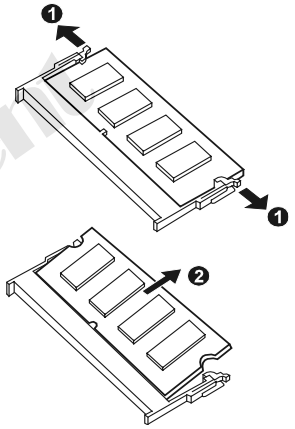

Figure 2-14 Remove the DDR-SDRAM

3. Pull the retaining clips outwards (❶) and remove the DDR-SDRAM (❷). (Figure 2-14)

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Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the DDR into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Tighten one screws to secure the DDR compartment cover to housing.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.7 Wireless Card

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (Refer to section 2.2.1 disassembly)
2. Loosen the two screws that secure the wireless card cover to the housing. (Figure 2-15)

Figure 2-15 Remove the Wireless card compartment cover

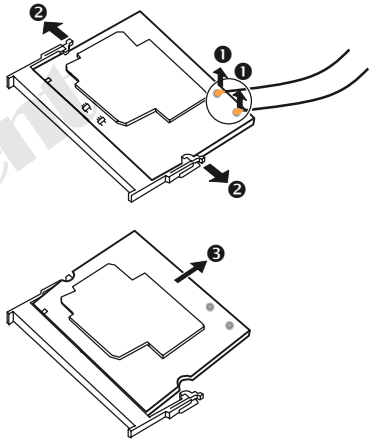

Figure 2-16 Remove the wireless card

3. Disconnect the wireless card's antennae first (❶). Then pull the retaining clips outwards (❷) and remove the wireless card (❸). (Figure 2-16)

Reassembly

1. To install the wireless card, match the wireless card 's notched part with the socket's projected part and firmly insert it into the socket. Then push down until the retaining clips lock the wireless card into position. Then sure that the antennae fully populated.
2. Tighten the screws to secure the wireless card compartment cover to the housing.
3. Replace the battery pack. (See section 2.2.1 reassembly)

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2.2.8 LCD Assembly

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (Refer to section 2.2.1 disassembly)
2. Remove the keyboard cover. (Refer to steps 1—3 of section 2.2.2 disassembly)
3. Remove the heatsink. (Refer to steps 1—3 of section 2.2.3 disassembly)
4. Disconnect the wireless card's antennae. (Refer to section 2.2.7 disassembly)
5. Open the top cover to level plane. Then remove the two hinge covers. And disconnect the two LCD cables from the system board. (Figure 2-17)

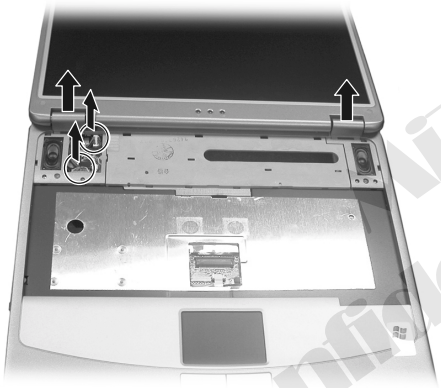

Figure 2-17 Remove two hinge covers and disconnect two cables

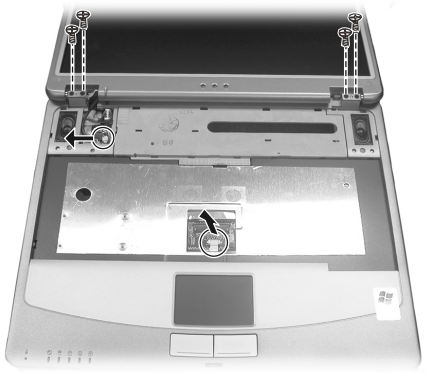

Figure 2-18 Loosen the screws and disconnect the cable

6. Remove the four screws of the hinges. Then disconnect the speaker's cord and touch pad cable. (Figure 2-18)

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7. Put the notebook upside down. Remove twenty- two screws that secure the housing. Then lift the housing from the rack. (Figure 2-19)

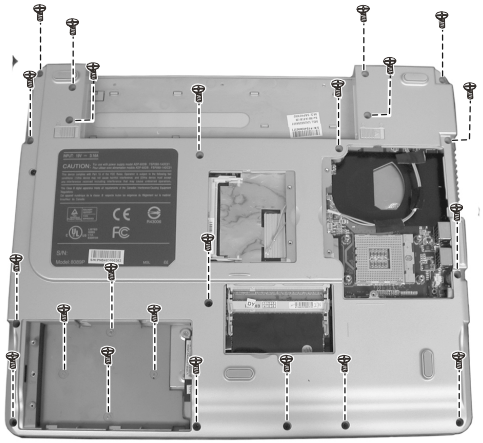

Figure 2-19 Remove the housing

Figure 2-20 Remove the screws

8. Remove two screws in the rear of the notebook. (Figure 2-20)

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9. To remove the modem card, loosen the screws and disconnect the cable. (Figure 2-21)

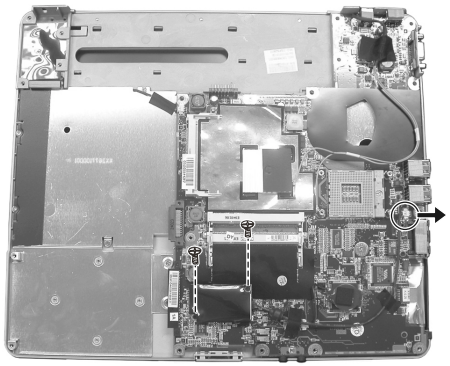

Figure 2-21 Remove the screws

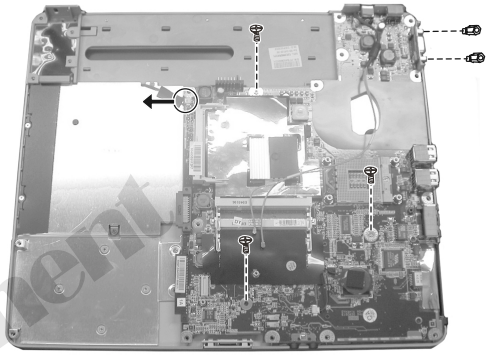

Figure 2-22 Remove the system board

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10. Remove the three screws and two hex nuts that secure the system board. And disconnect one cord. (Figure 2-22)

11. Free the wireless card's antennae wires. Separate the LCD ASSY away. (Figure 2-23)

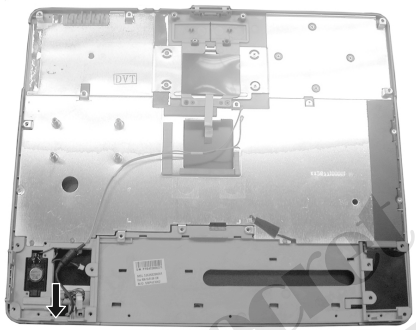

Figure 2-23 Separate the LCD ASSY

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Reassembly

1. Fit the LCD assembly and sure the wireless card's antennae wires no overlaid by top cover
2. Attach the system board and tighten the screws and hex nuts to secure the system board in the top cover. Then reconnect the cord
3. Fit the modem card and secure it with two screws. Then Reconnect the cable.
4. Replace the housing. Tighten all of screws to secure the housing.
5. Secure the LCD assembly with four screws of the hinges.
6. Reconnect the LCD cables、speaker cord and touch pad cable.
7. Replace two hinge covers.
8. Replace the heatsink 、keyboard cover and battery pack. (Refer to sections 2.2.1、 2.2.2 and 2.2.3 reassembly)

2.2.9 LCD Panel

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (Refer to section 2.2.1 disassembly)
2. Remove the keyboard cover. (Refer to steps 1—3 of section 2.2.2 disassembly)
3. Remove the heatsink. (Refer to steps 1—3 of section 2.2.3 disassembly)
4. Disconnect the wireless card's antennae. (Refer to section 2.2.7 disassembly)
5. Remove the LCD assembly. (See section 2.2.8 Disassembly.)
6. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-24)

Figure 2-24 Remove LCD frame

Figure 2-25 Remove LCD panel

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7. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
8. Remove the six screws on two sides of LCD panel, and disconnect the cable from the inverter board. (Figure 2-25)

9. Remove the four screws to remove the LCD bracket on side of the LCD panel. (Figure 2-26)

Figure 2-26 Remove the LCD bracket

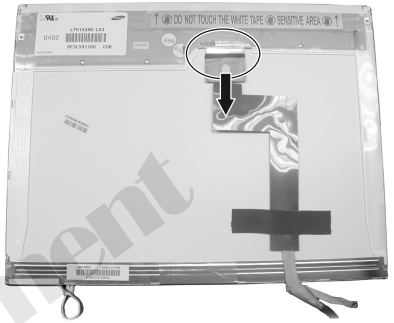

Figure 2-27 Remove the LCD wire

10. Disconnect the wire from bottom of the LCD panel. (Figure 2-27)

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Reassembly

1. Reconnect the wire to the LCD panel.
2. Attach the LCD bracket on the LCD panel and secure with four screws.
3. Fit the LCD panel back into place and secure with six screws, and reconnect the cable to the inverter board.
4. Fit the LCD cover back into the LCD housing. Tighten two screws to secure the LCD cover attach the rubber pads.
5. Replace the LCD assembly and battery pack. (See section 2.2.1and 2.2.7 reassembly.)

2.2.10 Inverter Board

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (Refer to section 2.2.1 disassembly)
2. Remove the keyboard cover. (Refer to steps 1—3 of section 2.2.2 disassembly)
3. Remove the heatsink. (Refer to steps 1—3 of section 2.2.3 disassembly)
4. Disconnect the wireless card's antennae. (Refer to section 2.2.7 disassembly)
5. Remove the LCD assembly. (See section 2.2.8 Disassembly.)
6. Remove the LCD cover. (Refer to steps 6-7 of section 2.2.9 disassembly.)
7. Remove two screws and disconnect the cables from the inverter board. (Figure 2-28)

Figure 2-28 Remove the Inverter Board

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Reassembly

1. Replace the inverter board and secure it with two screws.
2. Reconnect the inverter board cables.
3. Fit the LCD cover back into the LCD housing. Tighten two screws to secure the LCD cover attach the rubber pads.
4. Replace the LCD assembly and battery pack. (See section 2.2.1and 2.2.7 reassembly.)

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2.2.11 System Board

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (Refer to section 2.2.1 disassembly)
2. Remove the keyboard cover. (Refer to steps 1—3 of section 2.2.2 disassembly)
3. Remove the heatsink. (Refer to steps 1—3 of section 2.2.3 disassembly)
4. Disconnect the wireless card's antennae. (Refer to section 2.2.7 disassembly)
5. Open the top cover to level plane. Then remove the two hinge covers. And disconnect the two LCD cables from the system board. (Figure 2-29)

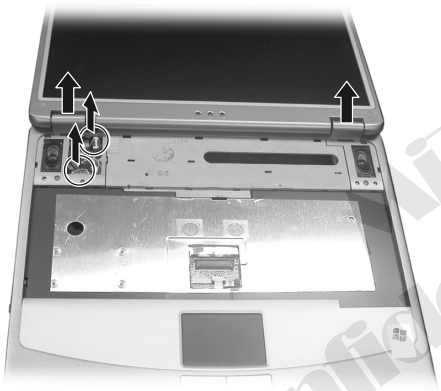

Figure 2-29 Remove two hinge covers and disconnect two cables

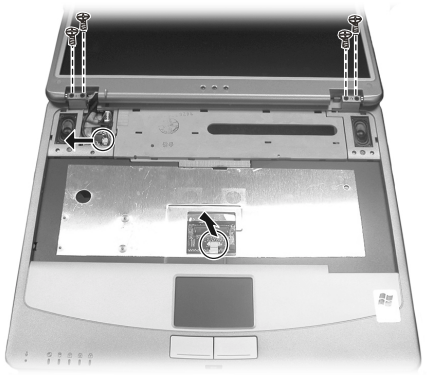

Figure 2-30 Loosen the screws and disconnect the cable

6. Remove the four screws of the hinges. Then disconnect the speaker's cord and touch pad cable. (Figure 2-30)

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7. Put the notebook upside down. Remove twenty- two screws that secure the housing. Then lift the housing from the rack. (Figure 2-31)

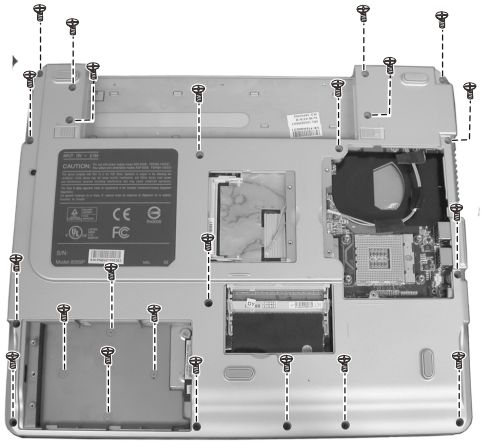

Figure 2-31 Remove the housing

Figure 2-32 Remove the screws

8. Remove two screws in the rear of the notebook. (Figure 2-32)

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9. To remove the modem card, loosen the two screws and disconnect the cable. (Figure 2-33)

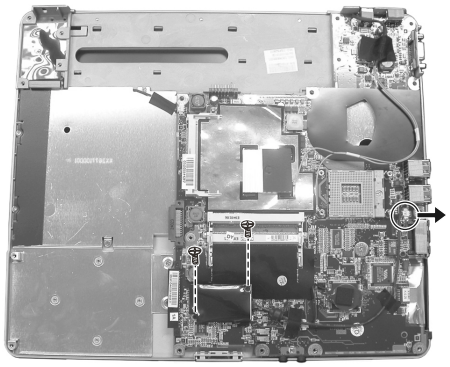

Figure 2-33 Remove the screws and hex nuts

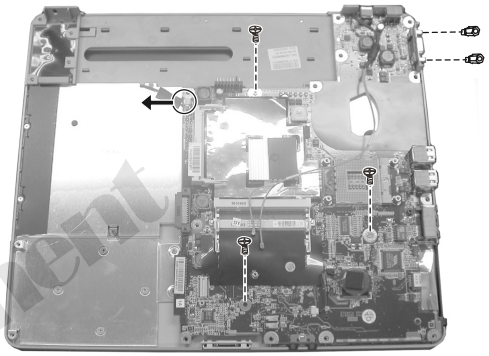

Figure 2-34 Remove the system board

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10. Remove the three screws and two hex nuts that secure the system board. And disconnect one cord. Now you can lift up the system board. (Figure 2-34)

Reassembly

1. Fit the system board and secure with three screws and two hex nuts.
2. Fit the modem and secure with two screws and reconnect the wire.
3. Replace the housing and secure with twenty-two screws.
4. Upturn the notebook. Take ulterior step to fasten the housing by two screws on the rear of the notebook.
5. Reconnect the touch pad's cable and speaker's cord.
6. Replace the battery pack, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly. (See the reassembly parts in previous sections.)

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2.2.12 Touch pad

Disassembly

1. Remove the system board. (See section 2.2.10disassembly)
2. Remove the two screws to lift up the touchpad button. (Figure 2-35)

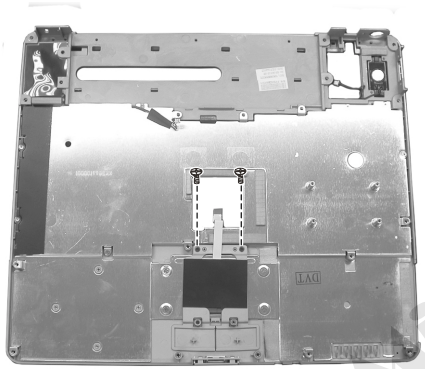

Figure 2-35 Remove the touch pad button

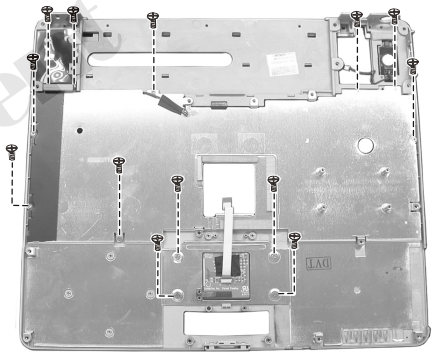

Figure 2-36 Remove the touchpad shield

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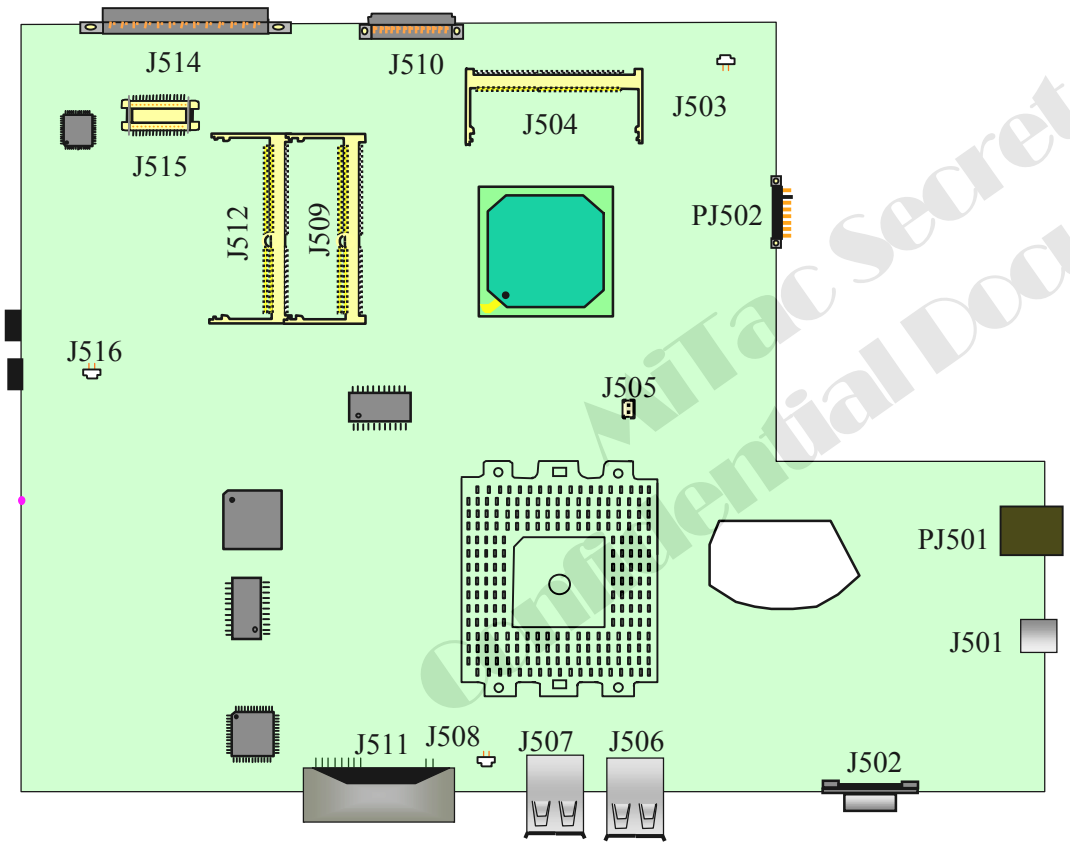
3. To tack the touchpad out, remove the thirteen screws that secure the touchpad shielding. (Figure 2-36)

Reassembly

1. Replace the touchpad and fit the touchpad shielding upon it and secure with thirteen screws.
2. Replace the touch pad button and secure with two screws.
3. Assemble the notebook. (See the reassembly parts in previous sections.)

3. Definition & Location of Connectors / Switches

3.1 Mother Board-A



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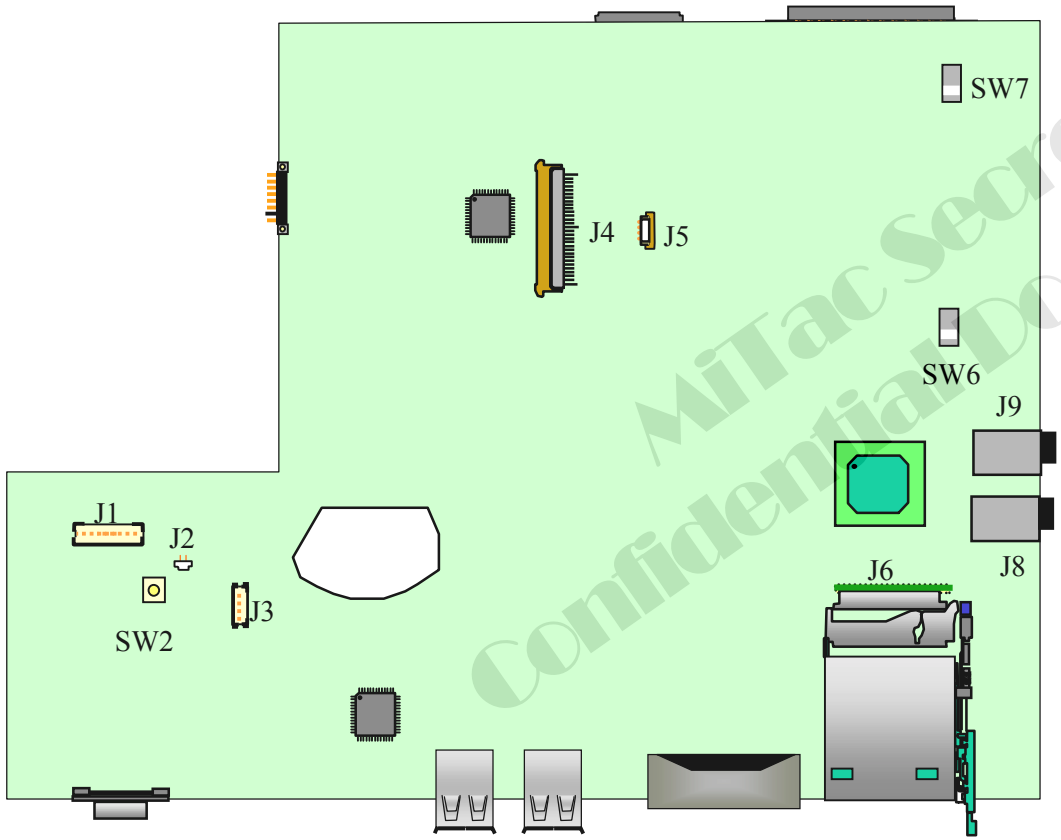
- J501 : S-TV Output Connector
- J502 : VGA Connector
- J503 : Internal Right Speaker Connector
- J504 : Mini PCI Slot
- J505 : CPU Fan Connector
- J506,J507 : USB Connector
- J508 : Modem Connector
- J509,J512 : SO DIMM Slot
- J510 : CD-ROM Connector
- J511 : RJ11/RJ45 Connector
- J514 : HDD Connector
- J515 : MDC Connector
- J516 : CMOS Battery Connector
- PJ501 : AC Adapter Jack
- PJ502 : Battery Connector

3. Definition & Location of Connectors / Switches

3.2 Mother Board-B



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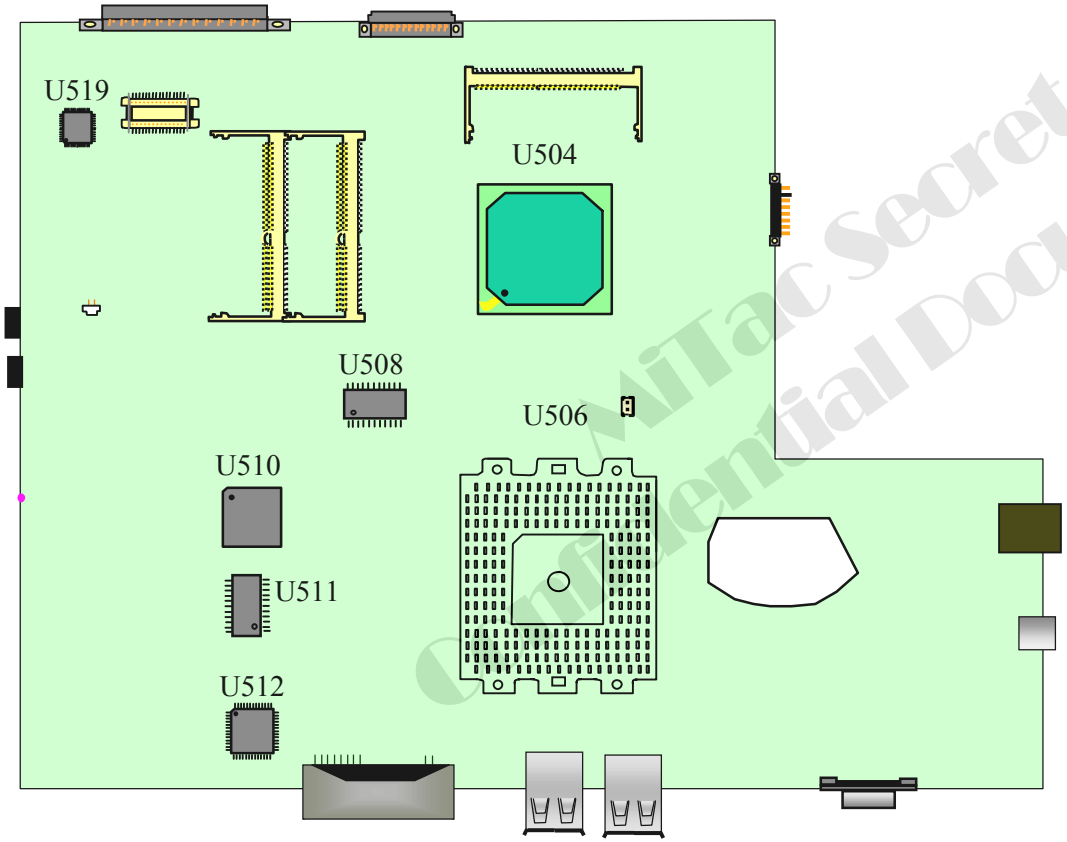
- J1 : LCD Connector
- J2 : Left Audio Channel Connector
- J3 : LCD Inverter Board Connector
- J4 : Internal Keyboard Connector
- J5 : Touch Pad Connector
- J6 : PC Card Slot
- J8 : Microphone Jack
- J9 : Audio Output Jack
- SW2 : H8 Power Button
- SW6 : SW_LEFT
- SW7 : SW_RIGHT

4. Definition & Location of Major Components

4.1 Mother Board-A



- U504 : Intel Monrata-GME
- U506 : Intel Banias CPU
- U508 : Clock Generator PLL207-1510C
- U510 : CB710 Card Bud Control&Reader
- U511 : LAN VT6105-L
- U512 : BIOS SST49LF004A
- U519 : Audio Codec ALC202

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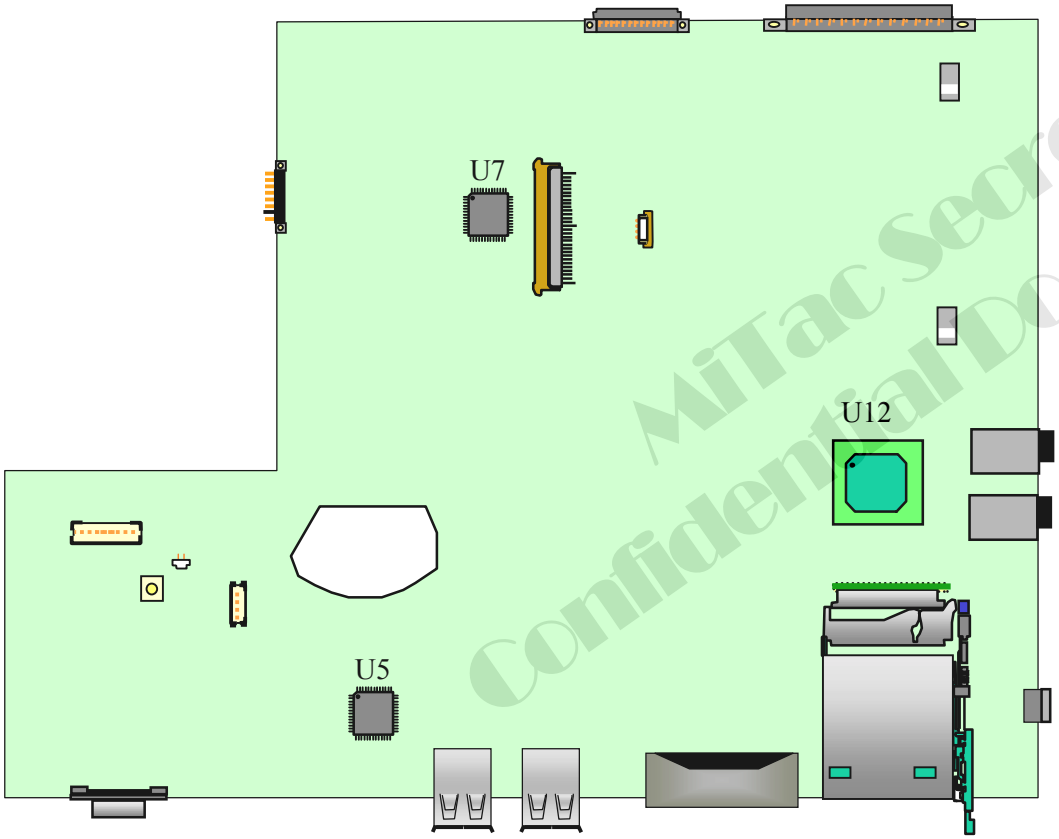
4. Definition & Location of Major Components

4.2 Mother Board-B



- U5 : TV Encoder CH7011A
- U7 : Winbond W83L950D
- U12 : Intel ICH4-M

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5. Pin Descriptions of Major Components

5.1 Intel Pentium M Processor

CPU Pin Description

`Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) define a 2 32 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel Pentium M processor system bus. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. Signals / Associated Strobe REQ[4:0]#, A[16:3]# / ADSTB[0]# A[31:17]# / ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:0]# **BPM[3]**	O I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.

CPU Pin Description Continue

Signal Name	Type	Description
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the MCH-M (High Priority Agent) of the Intel 855PM or Intel 855GM chipset.
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** Data Group / DSTBN#/DSTBP# / DINV# D[15:0]# / 0 / 0 D[31:16]# / 1 / 1 D[47:32]# / 2 / 2 D[63:48]# / 3 / 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.

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5.1 Intel Pentium M Processor

CPU Pin Description Continue

Signal Name	Type	Description
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DINV[3:0]# Assignment To Data Bus** Bus Signal / Data Bus Signals: DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the MCH-M component of the Intel 855PM or Intel 855GM chipset.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBN[0]# D[31:16]#, DINV[1]# — DSTBN[1]# D[47:32]#, DINV[2]# — DSTBN[2]# D[63:48]#, DINV[3]# — DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#

CPU Pin Description Continue

Signal Name	Type	Description
DPWR#	I	DPWR# is a control signal from the Intel 855PM and Intel 855GM chipsets used to reduce power on the Intel Pentium M data bus input buffers.
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

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5.1 Intel Pentium M Processor

CPU Pin Description Continue

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power on Reset vector configured during power on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep).

CPU Pin Description Continue

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
ITP_CLK[1:0]	I	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects. These are not processor signals.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	-	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.

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5.1 Intel Pentium M Processor

CPU Pin Description Continue

Signal Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3	I	TEST1, TEST2, and TEST3 must be left unconnected but should have a stuffing option connection to V SS separately using 1-k, pull-down resisitors.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

CPU Pin Description Continue

Signal Name	Type	Description
VCC	I	Processor core power supply.
VCCA[3:0]	I	VCCA provides isolated power for the internal processor core PLL's.
VCCP	I	Processor I/O Power Supply.
VCCQ[1:0]	I	Quiet power supply for on die COMP circuitry. These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.
VCCSENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations.
VSSSENSE	O	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise.

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5.2 Intel 82855GME Graphics and Memory Controller Hub (GMCH)

Host Interface Signal Descriptions

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase. The GMCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	I/O AGTL+	**Bus Request 0#:** The GMCH pulls the processor bus BREQ**0#** signal low during **CPURST#.** The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 BCLKs. BREQ0# should be tristated after the hold time requirement has been satisfied. During regular operation, the GMCH will use BREQ0# as an early indication for FSB Address and Ctl input buffer and sense amp activation.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts CPURST# while RESET# (PCIRST# from ICH4-M) is asserted and for approximately 1 ms after RESET# is deasserted. The CPURS**T#** allows the processor to begin execution in a known state. Note that the ICH4-M must provide CPU strap set-up and hold-times around CPURST#. This requires strict synchronization between GMCH, CPURST# deassertion and ICH4-M driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer:** GMCH will generate a deferred response as defined by the rules of the GMCH's Dynamic Defer policy. The GMCH will also use the DEFER# signal to indicate a CPU retry response.

Host Interface Signals Continue

Signal Name	Type	Description
DINV[3:0]#	I/O AGTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DINV# Data Bits** DINV[3]# HD[63:48]# DINV[2]# HD[47:32]# DINV[1]# HD[31:16]# DINV[0]# HD[16:0]#
DPSLP#	I CMOS	**Deep Sleep #:** This signal comes from the ICH4-M device, providing an indication of C3 and C4 state control to the CPU. Deassertion of this signal is used as an early indication for C3 and C4 wake up (to active HPLL). Note that this is a low-voltage CMOS buffer operating on the FSB VTT power plane.
DRDY#	I/O AGTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of Hub interface. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSTB[1:0]#	I/O AGTL+	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe Address Bits** HADSTB[0]# HA[16:3]#, HREQ[4:0]# HADSTB[1]# HA[31:17]#
HD[63:0]#	I/O AGTL+	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.

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5.2 Intel 82855GME Graphics and Memory Controller Hub (GMCH)

Host Interface Signal Descriptions (Continued)

Signal Name	Type	Description
HDSTBP[3:0]# **HDSTBN[3:0]#**	I/O AGTL+	**Differential Host Data Strobes:** The differential source synchronous strobes are used to **transfer HD[63:0]# and DINV[3:0]# at** the 4x transfer rate. **Strobe Data Bits** HDSTBP[3]#, HDSTBN[3]# HD[63:48]#, DINV[3]# HDSTBP[2]#, HDSTBN[2]# HD[47:32]#, DINV[2]# HDSTBP[1]#, HDSTBN[1]# HD[31:16]#, DINV[1]# HDSTBP[0]#, HDSTBN[0]# HD[15:0]#, DINV[0]#
HIT#	I/O AGTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I/O AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no Hub interface snoopable access to system memory is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the GMCH Host Bridge are defined in the Host Interface section of this document.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	O AGTL+	**Response Status:** Indicates the type of response according to the following the table: **RS[2:0]# Response type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by GMCH) 100 Hard Failure (not driven by GMCH) 101 No data response 110 Implicit Write back 111 Normal data response

DDR SDRAM Interface Descriptions

Signal Name	Type	Description
SCS[3:0]#	O SSTL_2	**Chip Select:** These pins select the particular DDR SDRAM components during the active state. **NOTE:** There is one SCS# per DDR-SDRAM Physical SO-DIMM device row. These signals can be toggled on every rising System Memory Clock edge (SCMDCLK).
SMA[12:0]	O SSTL_2	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to the DDR SDRAM.
SBA[1:0]	O SSTL_2	**Bank Select (Memory Bank Address):** These signals define which banks are selected within each DDR SDRAM row. The SMA and SBA signals combine to address every possible location within a DDR SDRAM device.
SRAS#	O SSTL_2	**DDR Row Address Strobe: SRAS#** may be heavily loaded and requires tw0 DDR SDRAM clock cycles for setup time to the DDR SDRAMs. Used with SCAS# and SWE# (along with SCS#) to define the system memory commands.
SCAS#	O SSTL_2	**DDR Column Address Strobe:** SCAS# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs. Used with SRAS# and SWE# (along with SCS#) to define the system memory commands.
SWE#	O SSTL_2	**Write Enable:** Used with SCAS# and SRAS# (along with SCS#) to define the DDR SDRAM commands. SWE# is asserted during writes to DDR SDRAM. SWE# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs.
SDQ[71:0]	I/O SSTL_2	**Data Lines:** These signals are used to interface to the DDR SDRAM data bus. **NOTE:** ECC error detection is supported: by the SDQ[71:64] signals.

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5.2 Intel 82855GME Graphics and Memory Controller Hub (GMCH)

DDR SDRAM Interface Descriptions (Continued)

Signal Name	Type	Description
SDQS[8:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS is centered on data. During reads, SDQS is edge aligned with data. The following list matches the data strobe with the data bytes. There is an associated data strobe (DQS) for each data signal (DQ) and check bit (CB) group. SDQS[7] -> SDQ[63:56] SDQS[6] -> SDQ[55:48] SDQS[5] -> SDQ[47:40] SDQS[4] -> SDQ[39:32] SDQS[3] -> SDQ[31:24] SDQS[2] -> SDQ[23:16] SDQS[1] -> SDQ[15:8] SDQS[0] -> SDQ[7:0] **NOTE:** ECC error detection is supported by the SDQS[8] signal.
SCKE[3:0]	O SSTL_2	**Clock Enable:** These pins are used to signal a self-refresh or power down command to the DDR SDRAM array when entering system suspend. SCKE is also used to dynamically power down inactive DDR SDRAM rows. There is one SCKE per DDR SDRAM row. These signals can be toggled on every rising SCK edge.
SMAB[5,4,2,1]	O SSTL_2	**Memory Address Copies:** These signals are identical to SMA[5,4,2,1] and are used to reduce loading for selective CPC(clock-per-command). These copies are not inverted.
SDM[8:0]	O SSTL_2	**Data Mask:** When activated during writes, the corresponding data groups in the DDR SDRAM are masked. There is one SDM for every eight data lines. SDM can be sampled on both edges of the data strobes. **NOTE:** ECC error detection is supported by the SDM[8] signal.
RCVENOUT#	O SSTL_2	**Clock Output:** Reserved, NC.
RCVENIN#	O SSTL_2	**Clock Input:** Reserved, NC.

AGP Addressing Signal Descriptions

Signal Name	Type	Description
GPIPE#	I AGP	**Pipelined Read:** This signal is asserted by the AGP master to indicate a full width address is to be enqueued on by the target using the **AD** bus. One address is placed in the AGP request queue on each rising clock edge while **PIPE#** is asserted. When **PIP**E# is deasserted no new requests are queued across the AD bus. **During SBA Operation:** This signal is **not used** if SBA (Side Band Addressing) is selected. **During FRAME# Operation:** This signal is **not used** during AGP FRAME# operation. **PIPE#** is a sustained tri-state signal from masters (graphics controller), and is an input to the GMCH.
GSBA[7:0]	I AGP	**Side-band Address:** These signals are used by the AGP master (graphics controller) to pass address and command to the GMCH. The **SBA** bus and AD bus operate independently. That is, transactions can proceed on the **SBA** bus and the AD bus simultaneously. **During PIPE# Operation:** These signals are **not used** during PIPE# operation. **During FRAME# Operation:** These signals are **not used** during AGP FRAME# operation. **NOTE:** When sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).

5 contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. The master may not switch methods without a full reset of the system. When PIPE# is used to queue addresses the master isnot allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism, but rather a static decision when the device is first being configured after reset

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5.2 Intel 82855GME Graphics and Memory Controller Hub (GMCH)

AGP Status Signal Descriptions

Signal Name	Type	Description		
GST[2:0]	O AGP	**Status:** Provides information from the arbiter to an AGP Master on what it may do. **ST[2:0]** only have meaning to the master when its **GNT#** is asserted. When **GNT#** is deasserted these signals have no meaning and must be gnored.	**ST[2:0**	**Meaning**
			000	Previously requested low priority read data is being returned to the master arbiter to an AGP
			001	Previously requested high priority read data is being returned to the master
			010	The master is to provide low priority write data for a previously queued write command
			011	The master is to provide high priority write data for a previously queued write command.
			100	Reserved
			101	Reserved
			110	Reserved
			111	The master has been given permission to start a bus transaction. The master may queue AGP requests by asserting **PIPE#** or start a PCI transaction by asserting **FRAME**#

AGP Flow Control Signals

Signal Name	Type	Description
GRBF#	I AGP	**Read Buffer Full:** Read buffer full indicates if the master is ready to accept previously requested low priority read data. When **RBF#** is asserted the GMCH is not allowed to initiate the return low priority read data. That is, the GMCH can finish returning the data for the request currently being serviced. **RBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.
GWBF#	I AGP	**Write-Buffer Full:** indicates if the master is ready to accept Fast Write data from the GMCH. When **WBF#** is asserted the GMCH is not allowed to drive Fast Write data to the AGP master. **WBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.

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5.2 Intel 82855GME Graphics and Memory Controller Hub (GMCH)

AGP/PCI Signals-Semantics Descriptions

Signal Name	Type	Description
GFRAME#	I/O AGP	**G_FRAME:** Frame. **During PIPE# and SBA Operation:** Not used by AGP SBA and PIPE# operations. **During Fast Write Operation:** Used to frame transactions as an output during Fast Writes. **During FRAME# Operation:** G_FRAME# is an output when the GMCH acts as an initiator on the AGP Interface. G_FRAME# is asserted by the GMCH to indicate the beginning and duration of an access. G_FRAME# is an input when the GMCH acts as a FRAME#-based AGP target. As a FRAME#-based AGP target, the GMCH latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which GMCH samples FRAME# active.
GIRDY#	I/O AGP	**G_IRDY#: Initiator Ready.** **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_IRDY# is an output when GMCH acts as a FRAME#-based AGP initiator and an input when the GMCH acts as a FRAME#-based AGP target. The assertion of G_IRDY# indicates the current FRAME#-based AGP bus initiator's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_IRDY# indicates that the AGP-compliant master is ready to provide all write data for the current transaction. Once G_IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The master is never allowed to insert a wait state during the initial data transfer (32 bytes) of a write transaction. However, it may insert wait states after each 32-byte block is transferred.

AGP Strobe Descriptions

Signal Name	Type	Description
GADSTB[0]	I/O AGP	**Address/Data Bus Strobe-0:** provides timing for 2x and 4x data on **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
GADSTB#[0]	I/O AGP	**Address/Data Bus Strobe-0 Complement:** With AD STB0, forms a differential strobe pair that provides timing information for the **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
GADSTB[1]	I/O AGP	**Address/Data Bus Strobe-1:** Provides timing for 2x and 4x data on **AD[31:16]** and **C/BE[3:2]#** signals. The agent that is providing the data will drive this signal.
GADSTB#[1]	I/O AGP	**Address/Data Bus Strobe-1 Complement:** With AD STB1, forms a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals in 4X mode. The agent that is providing the data will drive this signal.
GSBSTB	I AGP	**Sideband Strobe:** Provides timing for 2x and 4x data on the **SBA[7:0]** bus. It is driven by the AGP master after the system has been configured for 2x or 4x sideband address mode.
GSBSTB#	I AGP	**Sideband Strobe Complement:** The differential complement to the **SB_STB** signal. It is used to provide timing 4x mode.

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5.2 Intel 82855GME Graphics and Memory Controller Hub (GMCH)

AGP/PCI Signals-Semantics Descriptions (Continued)

Signal Name	Type	Description
GTRDY#	I/O AGP	**G_TRDY#:** Target Ready. **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_TRDY# is an input when the GMCH acts as an AGP initiator and is an output when the GMCH acts as a FRAME#-based AGP target. The assertion of G_TRDY# indicates the target's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_TRDY# indicates the AGP-compliant target is ready to receive write data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on write transactions.
GSTOP#	I/O AGP	**G_STOP#:** Stop. **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_STOP# is an input when the GMCH acts as a FRAME#-based AGP initiator and is an output when the GMCH acts as a FRAME#-based AGP target. G_STOP# is used for disconnect, retry, and abort sequences on the AGP interface.
GDEVSEL#	I/O AGP	**G_ DEVSEL#: Device Select.** **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_DEVSEL#, when asserted, indicates that a FRAME#-based AGP target device has decoded its address as the target of the current access. The GMCH asserts G_DEVSEL# based on the DDR SDRAM address range being accessed by a PCI initiator. As an input, G_DEVSEL# indicates whether the AGP master has recognized a PCI cycle to it.
GREQ#	I AGP	**G_REQ#:** Request. **During SBA Operation:** This signal is not used during SBA operation. **During PIPE# and FRAME# Operation:** G_REQ#, when asserted, indicates that the AGP master is requesting use of the AGP interface to run a FRAME#- or PIPE#-based operation.
GGNT#	O AGP	**G_GNT#: Grant.** **During SBA, PIPE# and FRAME# Operation:** G_GNT#, along with the information on the ST[2:0] signals (status bus), indicates how the AGP interface will be used next. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings.
GAD[31:0]	I/O AGP	**G_AD[31:0]: Address/Data Bus.** **During PIPE# and FRAME# Operation:** The G_AD[31:0] signals are used to transfer both address and data information on the AGP interface. **During SBA Operation:** The G_AD[31:0] signals are used to transfer data on the AGP interface.
GCBE#[3:0]	I/O AGP	**Command/Byte Enable.** **During FRAME# Operation:** During the address phase of a transaction, the G_CBE[3:0]# signals define the bus command. During the data phase, the G_CBE[3:0]# signals are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The commands issued on the G_CBE# signals during FRAME#-based AGP transactions are the same G_CBE# command described in the PCI 2.2 specification. **During PIPE# Operation:** When an address is enqueued using PIPE#, the C/BE# signals carry command information. The command encoding used during PIPE#-based AGP is *different* than the command encoding used during FRAME#-based AGP cycles (or standard PCI cycles on a PCI bus). **During SBA Operation:** These signals are not used during SBA operation.
GPAR	I/O AGP	**Parity.** **During FRAME# Operation:** G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP target during each data phase of a FRAME#-based AGP memory read cycle. Even parity is generated across G_AD[31:0] and G_CBE[3:0]#. **During SBA and PIPE# Operation:** This signal is not used during SBA and PIPE# operation.

PCIRST# from the ICH4-M is assumed to be connected to RSTIN# and is used to reset AGP interface logic within the GMCH. The AGP agent will also typically use PCIRST# provided by the ICH4-M as an input to reset its internal logic.

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5.2 Intel 82855GME Graphics and Memory Controller Hub (GMCH)

Hub Interface Signals

Signal Name	Type	Description
HL[10:0]	I/O Hub	**Packet Data:** Data signals used for HI read and write operations.
HLSTB	I/O Hub	**Packet Strobe:** One of two differential strobe signals used to transmit or receive packet data over HI.
HLSTB#	I/O Hub	**Packet Strobe Complement**: One of two differential strobe signals used to transmit or receive packet data over HI.

Dedicated LVDS LCD Flat Panel Interface Signal Descriptions

Name	Type	Voltage	Description
ICLKAP	O LVDS	1.25 V± 225 mV	**Channel A differential clock pair output (true):** 245-800 MHz
ICLKAM	O LVDS	1.25 V±225 mV	**Channel A differential clock pair output (compliment):** 245-800 MHz.
IYAP[3:0]	O LVDS	1.25 V±225 mV	**Channel A differential data pair 3:0 output (true):** 245-800MHz.
IYAM[3:0]	O LVDS	1.25 V±225 mV	**Channel A differential data pair 3:0 output (compliment):** 245-800 MHz.
ICLKBP	O LVDS	1.25 V±225 mV	**Channel B differential clock pair output (true):** 245-800 MHz.
ICLKBM	O LVDS	1.25 V±225 mV	**Channel B differential clock pair output (compliment):** 245-800 MHz.
IYBP[3:0]	O LVDS	1.25 V±225 mV	**Channel B differential data pair 3:0 output (true):** 245-800MHz.
IYBM[3:0]	O LVDS	1.25 V± 225 mV	**Channel B differential data pair 3:0 output (compliment):** 245-800 MHz.

Digital Video Output B (DVOB) Port Signal Descriptions

Name	Type	Description
DVOBD[11:0]	O DVO	**DVOB Data:** This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOBCLK and DVOBCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the lower 12-bits of pixel data. DVOBD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOBHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOB interface. **DVOBHSYNC** should be left as left as NC (“Not Connected”) if not used.
DVOBVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOB interface. DVOBVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOBBLANK#	O DVO	**Flicker Blank or Border Period Indication: DVOBBLANK# is** a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOBBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOBFLDSTL	I DVO	**TV Field and Flat Panel Stall Signa**l. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOB TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOB Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOBFLDSTL needs to be pulled down if not used.

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5.2 Intel 82855GME Graphics and Memory Controller Hub (GMCH)

DVOB and DVOC Port Common Signal Descriptions

Name	Type	Description
DVOBCINTR#	I DVO	**DVOBC Interrupt**: This pin is used to signal an interrupt, typically used to indicate a hot plug or unplug of a digital display.
ADDID[7:0]	I DVO	**ADDID[7:0]**: These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. **Note**: Bit[7] needs to be strapped low when an on-board DVO device is present. The other pins should be left as NC.
DVODETECT	I DVO	**DVODETECT**: This strapping signal indicates to the GMCH whether a DVO device is present or not. When a DVO device is connected, then DVODETECT = 0.

Analog CRT Display Signal Descriptions

Pin Name	Type	Description
VSYNC	O CMOS	**CRT Vertical Synchronization**: This signal is used as the vertical sync signal.
HSYNC	O CMOS	**CRT Horizontal Synchronization**: This signal is used as the horizontal sync signal.
RED	O Analog	**Red (Analog Video Output)**: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-§Ù equivalent load on each pin (e.g., 75-§Ù resistor on the board, in parallel with the 75-§Ù CRT load).
RED#	O Analog	**Red# (Analog Output):** Tied to ground.
GREEN	O Analog	**Green (Analog Video Output)**: This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5-§Ù equivalent load on each pin (e.g.,75-§Ù resistor on the board, in parallel with the 75- §Ù CRT load).
GREEN#	O Analog	**Green# (Analog Output):** Tied to ground.
BLUE	O Analog	**Blue (Analog Video Output)** : This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-§Ù equivalent load on each pin (e.g., 75- ohm resistor on the board, in parallel with the 75-§Ù CRT load).
BLUE#	O Analog	**Blue# (Analog Output):** Tied to ground.

Digital Video Output C (DVOC) Port Signal Descriptions

Name	Type	Description
DVOCD[11:0]	O DVO	**DVOC Data**: This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOCCLK and DVOCCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the upper 12-bits of pixel data. DVOCD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOCHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOC interface. DVOCHSYNC should be left as left as NC (“Not Connected”) if not used.
DVOCVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOC interface. DVOCVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOCBLANK#	O DVO	**Flicker Blank or Border Period Indication**: **DVOCBLANK#** is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOCBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOCFLDSTL	I DVO	**TV Field and Flat Panel Stall Signal**. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOC TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOC Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOCFLDSTL needs to be pulled down if not used.

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5.2 Intel 82855GME Graphics and Memory Controller Hub (GMCH)

GPIO Signal Descriptions

GPIO I/F Total	Type	Comments
RSTIN#	I CMOS	**Reset:** Primary Reset, Connected to PCIRST# of ICH4-M.
PWROK	I CMOS	**Power OK**: Indicates that power to GMCH is stable.
AGPBUSY#	O CMOS	**AGPBUSY:** Output of the GMCH IGD to the ICH4-M, which indicates that certain graphics activity is taking place. It will indicate to the ACPI software not to enter the C3 state. It will also cause a C3/C4 exit if C3/C4 was being entered, or was already entered when AGPBUSY# went active. Not active when the IGD is in any ACPI state other than D0.
EXTTS_0	I CMOS	**External Thermal Sensor Input:** This signal is an active low input to the GMCH and is used to monitor the thermal condition around the system memory and is used for triggering a read throttle. The GMCH can be optionally programmed to send a SERR, SCI, or SMI message to the ICH4-M upon the triggering of this signal.
LCLKCTLA	O CMOS	**SSC Chip Clock Control:** Can be used to control an external clock chip with SSC control.
LCLKCTLB	O CMOS	**SSC Chip Data Control:** Can be used to control an external clock chip for SSC control.
PANELVDDEN	O CMOS	**LVDS LCD Flat Panel Power Control:** This signal is used enable power to the panel interface.
PANELBKLTEN	O CMOS	**LVDS LCD Flat Panel Backlight Enable:** This signal is used to enable the backlight inverter (BLI)
PANELBKLTCTL	O CMOS	**LVDS LCD Flat Panel Backlight Brightness Control:** This signal is used as the Pulse Width Modulated (PWM) control signal to control the backlight inverter.
DDCACLK	I/O CMOS	**CRT DDC Clock:** This signal is used as the DDC clock signal between the CRT monitor and the GMCH.
DDCADATA	I/O CMOS	**CRT DDC Data:** This signal is used as the DDC data signal between the CRT monitor and the GMCH.
DDCPCLK	I/O CMOS	**Panel DDC Clock:** This signal is used as the DDC clock signal between the LFP and the GMCH.
DDCPDATA	I/O CMOS	**Panel DDC Data:** This signal is used as the DDC data signal between the LFP and the GMCH.

GPIO I/F Total	Type	Comments
MI2CCLK	I/O DVO	**DVO I2C Clock:** This signal is used as the I2C_CLK for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MI2CDATA	I/O DVO	**DVO I2C Data:** This signal is used as the I2C_DATA for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MDVICLK	I/O DVO	**DVI DDC Clock:** This signal is used as the DDC clock for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDVIDATA	I/O DVO	**DVI DDC Data:** The signal is used as the DDC data for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDDCDATA	I/O DVO	**DVI DDC Clock:** The signal is used as the DDC data for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.
MDDCCLK	I/O DVO	**DVI DDC Data:** The signal is used as the DDC clock for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Hub Interface Signals

Signal Name	Type	Description
HI[11:0]	I/O	**Hub Interface Signals**
HI_STB/HI_STBS	I/O	**Hub Interface Strobe/ Hub Interface Strobe Second:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the second of the two strobe signals.
HI_STB#/ HI_STBF	I/O	**Hub Interface Strobe Complement / Hub Interface Strobe First:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the first of the two strobe signals.
HICOMP	I/O	**Hub Interface Compensation:** Used for hub interface buffer compensation.
HI_VSWING	I	**Hub Interface Voltage Swing:** Analog input used to control the voltage swing and impedance strength of hub interface pins.

LAN Connect Interface Signals

Signal Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** Driven by the LAN Connect component. Frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The LAN Connect component uses these signals to transfer data and control information to the integrated LAN Controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data**: The integrated LAN Controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

EEPROM Interface Signals

Signal Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Clock**: Serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data In**: Transfers data from the EEPROM to the ICH3. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Out**: Transfers data from the ICH3 to the EEPROM.
EE_CS	O	**EEPROM Chip Select**: Chip select signal to the EEPROM.

Firmware Hub Interface Signals

Signal Name	Type	Description
FWH[3:0]/ LAD[3:0]	I/O	**Firmware Hub Signals.** Muxed with LPC address signals.
FWH[4]/ LFRAME#	I/O	LFRAME# **Firmware Hub Signals.** Muxed with LPC LFRAME# signal.

PCI Interface Signals

Signal Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The ICH4 drives all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0 0 0 0 Interrupt Acknowledge 0 0 0 1 Special Cycle 0 0 1 0 I/O Read 0 0 1 1 I/O Write 0 1 1 0 Memory Read 0 1 1 1 Memory Write 1 0 1 0 Configuration Read 1 0 1 1 Configuration Write 1 1 0 0 Memory Read Multiple 1 1 1 0 Memory Read Line 1 1 1 1 Memory Write and Invalidate All command encodings not shown are reserved. The ICH4 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select:** The ICH4 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH4 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH4 address or an address destined for the hub interface (main memory or AGP). As an input, DEVSEL# indicates the response to an ICH4-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the ICH4 until driven by a Target device.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

PCI Interface Signals (Continue)

Signal Name	Type	Description
FRAME#	I/O	**Cycle Frame:** The current Initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the Initiator asserts FRAME#, data transfers continue. When the Initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH4 when the ICH4 is the Target, and FRAME# is an output from the ICH4 when the ICH4 is the Initiator. FRAME# remains tri- stated by the ICH4 until driven by an Initiator.
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ICH4's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH4 has valid data present on AD[31:0]. During a read, it indicates the ICH4 is prepared to latch data. IRDY# is an input to the ICH4 when the ICH4 is the Target and an output from the ICH4 when the ICH4 is an Initiator. IRDY# remains tri-stated by the ICH4 until driven by an Initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the ICH4's ability, as a Target, to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH4, as a Target, has placed valid data on AD[31:0]. During a write, TRDY# indicates that the ICH4, as a Target, is prepared to latch data. TRDY# is an input to the ICH4 when the ICH4 is the Initiator and an output from the ICH4 when the ICH4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the ICH4 until driven by a target.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH4 counts the number of 1s within the 36 bits plus PAR and the sum is always even. The ICH4 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH4 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH4 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH4 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH4 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. ICH4 checks parity when it is the Target of a PCI write transaction. If a parity error is detected, the ICH4 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

PCI Interface Signals (Continue)

Signal Name	Type	Description
STOP#	I/O	**Stop:** STOP# indicates that the ICH4, as a Target, is requesting the Initiator to stop the current transaction. STOP# causes the ICH4, as an Initiator, to stop the current transaction. STOP# is an output when the ICH4 is a Target and an input when the ICH4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by the ICH4.
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The ICH4 drives PERR# when it detects a parity error. The ICH4 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[4:0]# **REQ[5]#/** REQ[B]#/ GPIO[1]	I	**PCI Requests:** The ICH4 supports up to 6 masters on the PCI bus. REQ[5]# is muxed with PC/PCI REQ[B]# (must choose one or the other, but not both). If not used for PCI or PC/PCI, REQ[5]#/REQ[B]# can instead be used as GPIO[1]. **NOTE:** REQ[0]# is programmable to have improved arbitration latency for for supporting PCI-based 1394 controllers.
GNT[4:0]# **GNT[5]#/** GNT[B]#/ GPIO[17]	O	**PCI Grants:** The ICH4 supports up to 6 masters on the PCI bus. GNT[5]# is muxed with PC/PCI GNT[B]# (must choose one or the other, but not both). If not needed for PCI or PC/PCI, GNT[5]# can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT[B]#/GNT[5]#/GPIO[17] has an internal pull-up.
PCICLK	I	**PCI Clock:** This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus. **NOTE:** This clock does not stop based on STP_PCI# signal. PCICLK only stops based on SLP_S1# or SLP_S3#.
PCIRST#	O	**PCI Reset:** ICH4 asserts PCIRST# to reset devices that reside on the PCI bus. The ICH4 asserts PCIRST# during power-up and when S/W initiates a hard reset sequence through the RC (CF9h) register. The ICH4 drives PCIRST# inactive a minimum of 1 ms after PWROK is driven active. The ICH4 drives PCIRST# active a minimum of 1 ms when initiated through the RC register.
PLOCK#	I/O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH4 asserts PLOCK# when it performs non- exclusive transactions on the PCI bus. Devices on the PCI bus (other than the ICH4) are not permitted to assert the PLOCK# signal.
SERR#	I/OD	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH4 has the ability to generate an NMI, SMI#, or interrupt.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

PCI Interface Signals (Continue)

Signal Name	Type	Description
PME#	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1-M–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH4 may drive PME# active due to an internal wake event. The ICH4 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.
CLKRUN#	I/O	**PCI Clock Run:** Used to support PCI Clock Run protocol. Connects to PCI devices that need to request clock re-start, or prevention of clock stopping. **NOTE:** An external pull-up to the core power plane is required.
REQ[A]#/ GPIO[0] **REQ[B]#/** REQ[5]#/ GPIO[1]	I	**PC/PCI DMA Request [A:B]:** This request serializes ISA-like DMA Requests for the purpose of running ISA-compatible DMA cycles over the PCI bus. This is used by devices such as PCI based Super I/O or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI requests, these signals can be used as General Purpose Inputs. REQ[B]# can instead be used as the 6th PCI bus request.
GNT[A]#/ GPIO[16] **GNT[B]#/** GNT[5]#/ GPIO[17]	O	**PC/PCI DMA Acknowledges [A: B]:** This grant serializes an ISA-like DACK# for the purpose of running DMA/ISA Master cycles over the PCI bus. This is used by devices such as PCI based Super/IO or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI, these signals can be used as General Purpose Outputs. GNTB# can also be used as the 6th PCI bus master grant output. These signal have internal pull-up resistors.

IDE Interface Signals

Signal Name	Type	Description
PDCS1#, SDCS1#	O	**Primary and Secondary IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDCS3#, SDCS3#	O	**Primary and Secondary IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDA[2:0], SDA[2:0]	O	**Primary and Secondary IDE Device Address:** These output signals are connected to the corresponding signals on the primary or secondary IDE connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.

IDE Interface Signals (Continue)

Signal Name	Type	Description
PDD[15:0], SDD[15:0]	I/O	**Primary and Secondary IDE Device Data:** These signals directly drive the corresponding signals on the primary or secondary IDE connector. There is a weak internal pull-down resistor on PDD[7] and SDD[7].
PDDREQ, SDDREQ	I	**Primary and Secondary IDE Device DMA Request:** These input signals are directly driven from the DRQ signals on the primary or secondary IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on these signals.
PDDACK#, SDDACK#	O	**Primary and Secondary IDE Device DMA Acknowledge:** These signals directly drive the DAK# signals on the primary and secondary IDE connectors. Each is asserted by the ICH4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
PDIOR#/ (PDWSTB/PRDMARDY#) **SDIOR#/** (SDWSTB/SRDMARDY#)	O	**Primary and Secondary Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may drive data onto the PDD or SDD lines. Data is latched by the ICH4 on the deassertion edge of PDIOR# or SDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH4 drives valid data on rising and falling edges of PDWSTB or SDWSTB. Primary and Secondary Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH4 deasserts PRDMARDY# or SRDMARDY# to pause burst data transfers.
PDIOW#/ (PDSTOP) **SDIOW#/** (SDSTOP)	O	**Primary and Secondary Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may latch data from the PDD or SDD lines. Data is latched by the IDE device on the deassertion edge of PDIOW# or SDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Stop (Ultra DMA): ICH4 asserts this signal to terminate a burst.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

IDE Interface Signals (Continue)

Signal Name	Type	Description
PIORDY#/ (PDRSTB/PWDMARDY#) **SIORDY#/** (SDRSTB/SWDMARDY#)	I	**Primary and Secondary I/O Channel Ready (PIO):** This signal will keep the strobe active (PDIOR# or SDIOR# on reads, PDIOW# or SDIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers. Primary and Secondary Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, the ICH4 latches data on rising and falling edges of this signal from the disk. Primary and Secondary Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.

Interrupt Signals

Signal Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]#/ GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IRQ[14:15]	I	**Interrupt Request 14:15:** These interrupt inputs are connected to the IDE drives. IRQ14 is used by the drives connected to the Primary controller and IRQ15 is used by the drives connected to the Secondary controller.
APICCLK	I	**APIC Clock:** This clock operates up to 33.33 MHz.
APICD[1:0]	I/OD	**APIC Data:** These bi-directional open drain signals are used to send and receive data over the APIC bus. As inputs the data is valid on the rising edge of APICCLK. As outputs, new data is driven from the rising edge of the APICCLK.

LPC Interface Signals

Signal Name	Type	Description
LAD[3:0]/ FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For the LAD[3:0] signals, internal pull-ups are provided.
LFRAME#/ FWH[4]	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[1:0]#	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals.

USB Interface Signals

Signal Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port 1:0 Differential:** These differential pairs are used to transmit data/address/command signals for ports 0 and 1. These ports can be routed to USB UHCI Controller #1 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port 3:2 Differential:** These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to USB UHCI Controller #2 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP4N	I/O	**Universal Serial Bus Port 5:4 Differential:** These differential pairs are used to transmit data/address/command signals for ports 4 and 5. These ports can be routed to USB UHCI Controller #3 or the USB EHCI Controller **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
OC[5:0]#	I/O	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor to ground. USBRBIAS should be connected to USBRBIAS# as close to the resistor as possible.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor to ground. USBRBIAS# should be connected to USBRBIAS as close to the resistor as possible.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Power Management Interface Signals

Signal Name	Type	Description
THRM#	I	**Thermal Alarm:** This is an active low signal generated by external hardware to start the hardware clock throttling mode. The signal can also generate an SMI# or an SCI.
THRMTRIP#	I	**Thermal Trip:** When low, THRMTRIP# indicates that a thermal trip from the processor occurred; the ICH4 will immediately transition to a S5 state. The ICH4 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S1#	O	**S1 Sleep Control:** SLP_S1# provides Clock Synthesizer or Power plane control. Optional use is to shut off power to non-critical systems when in the S1- M (Powered On Suspend), S3 (Suspend To RAM), S4 (Suspend to Disk) or S5 (Soft Off) states.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. It shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** SLP_S4# is for power plane control. It shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. The signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH4 that core power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH4 asserts PCIRST#. **NOTE:** PWROK must deassert for a minimum of 3 RTC clock periods for the ICH4 to fully reset the power and properly generate the PCIRST# output
PWRBTN#	I	**Power Button:** The Power Button causes SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal causes a wake event. If PWRBTN# is pressed for more than 4 seconds, this causes an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override occurs even if the system is in the S1-M–S4 states. This signal has an internal pull-up resistor.
RI#	I	**Ring Indicate:** This signal is an input from the modem interface. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Reset:** This pin forces an internal reset after being debounced. The ICH4 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.

Power Management Interface Signals Continue

Signal Name	Type	Description
LAN_RST#	I	**LAN Reset:** This signal must be asserted at least 10 ms after the resume well power (VccLAN3_3 and VccLAN1_5 is valid. When deasserted, this signal is an indication that the resume well power is stable.
SUS_STAT#/ LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH4 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.
C3_STAT#	O	**C3_STAT#:** This signal will typically be configured as C3_STAT#. It is used for indicating to an AGP device that a C3 state transition is beginning or ending. If C3_STAT# functionality is not required, this signal may be used as a GPO. **NOTE:** This signal will be asserted in S1-M on the ICH4-M.
SUSCLK	O	**Suspend Clock:** Output of the RTC generator circuit to use by other chips for refresh clock.
AGPBUSY#	I	**AGP Bus Busy:** To support the C3 state. This signal is an indication that the AGP device is busy. When this signal is asserted, the BM_STS bit will be set. If this functionality is not needed, this signal may be configured as a GPI.
STP_PCI#	O	**Stop PCI Clock:** This signal is an output to the external clock generator for it to turn off the PCI clock. Used to support PCI CLKRUN# protocol. If this functionality is not needed, This signal can be configured as a GPO.
STP_CPU#	O	**Stop CPU Clock:** Output to the external clock generator for it to turn off the processor clock. Used to support the C3 state. If this functionality is not needed, this signal can be configured as a GPO.
BATLOW#	I	**Battery Low:** This signal is an input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S1-M–S5 state. Can also be enabled to cause an SMI# when asserted.
CPUPERF#	OD	**CPU Performance:** CPUPERF# is used for Intel SpeedStep technology support. The signal selects which power state to put the processor in.
SSMUXSEL	O	**SpeedStep Mux Select:** SSMUXSEL is used for Intel SpeedStep technology support. The signal selects the voltage level for the processor.
VGATE/ VRMPWRGD	I	**VGATE/VRM Power Good:** VGATE/VRMPWRGD is used for Intel SpeedStep technology support. This is an output from the processor's voltage regulator to indicate that the voltage is stable. This signal may go inactive during an Intel SpeedStep transition.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Power Management Interface Signals (Continue)

Signal Name	Type	Description
DPRSLPVR	O	**Deeper Sleep - Voltage Regulator:** This signal is used to lower the voltage of VRM during C4 and S1-M states. When the signal is high, the voltage regulator outputs the lower "Deeper Sleep" voltage. When the signal is low (default), the voltage regulator outputs the higher "Normal" voltage. During PCIRST#, the output driver is disabled and an internal pull-down is enabled. This is needed for implementing a strap on the pin. When PCIRST# deasserts, the output driver is enabled. To guarantee no glitches on the DPRSLPVR pin, the pull-down is disabled after the output driver is fully enabled. **NOTE:** DPRSLPVR is sampled at the rising edge of PWROK as a functional strap.

Processor Interface Signals

Signal Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active. **Speed Strap:** During the reset sequence, ICH4 drives A20M# high if the corresponding bit is set in the FREQ_STRP register.
CPUSLP#	O	**CPU Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The ICH4 can optionally assert the CPUSLP# signal when going to the S1-M state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is asserted, the ICH4 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the General Control Register bit setting.
INTR	O	**CPU Interrupt:** INTR is asserted by the ICH4 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low. **Speed Strap:** During the reset sequence, ICH4 drives INTR high if the corresponding bit is set in the FREQ_STRP register.

Processor Interface Signals (Continue)

Signal Name	Type	Description
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **Speed Strap:** During the reset sequence, ICH4 drives IGNNE# high if the corresponding bit is set in the FREQ_STRP register.
INIT#	O	**Initialization:** INIT# is asserted by the ICH4 for 16 PCI clocks to reset the processor. ICH4 can be configured to support CPU BIST. In that case, INIT# will be active when PCIRST# is active.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH4 can generate an NMI when either SERR# or IOCHK# is asserted. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. **Speed Strap:** During the reset sequence, ICH4 drives NMI high if the corresponding bit is set in the FREQ_STRP register.
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH4's other sources of INIT#. When the ICH4 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH4 ignores RCIN# assertion during transitions to the S1-M, S3, S4 and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other PCIsets.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Processor Interface Signals (Continued)

Signal Name	Type	Description
CPUPWRGD	OD	**CPU Power Good:** This signal should be connected to the processor's PWRGOOD input. To allow for Intel ® SpeedStep™ technology support, this signal is kept high during an Intel SpeedStep technology state transition to prevent loss of processor context. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the ICH4's PWROK and VGATE / VRMPWRGD signals.
DPSLP#	O	**Deeper Sleep:** This signal is asserted by the ICH4 to the processor. When the signal is low, the processor enters the Deeper Sleep state by gating off the processor Core clock inside the processor. When the signal is high (default), the processor is not in the Deeper Sleep state. This signal behaves identically to the STP_CPU# signal, but at the processor voltage level.

SMBus Interface Signals

Signal Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up is required.
SMBALERT#/ GPIO[11]	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.

System Management Interface Signals

Signal Name	Type	Description
INTRUDER#	I	**Intruder Detect:** Can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK[0] corresponds to an SMBus Clock signal, and SMLINK[1] corresponds to an SMBus Data signal.

Real Time Clock Interface Signals

Signal Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal.

Other Clock Signals

Signal Name	Type	Description
CLK14	I	**Oscillator Clock:** Used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK48	I	**48 MHz Clock:** This clock is used to run the USB controller. It runs at 48 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK66	I	**66 MHz Clock:** This is used to run the hub interface. It runs at 66 MHz. This clock is permitted to stop during S1-M (or lower) states.

Miscellaneous Signals

Signal Name	Type	Description
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PCIRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well and sets the RTC_PWR_STS bit (bit 2 in GEN_PMCON3 register). **NOTES:** 1. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. 2. Unless entering the XOR Chain Test Mode, the RTCRST# input must always be high when all other RTC power planes are on.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

AC'97 Link Signals

Signal Name	Type	Description
AC_RST#	O	**AC '97 Reset:** This signal is a master hardware reset to external Codec(s).
AC_SYNC	O	**AC '97 Sync:** This signal is a 48 kHz fixed rate sample sync to the Codec(s).
AC_BIT_CLK	I	**AC97 Bit Clock:** This signal is a 12.288 MHz serial data clock generated by the external Codec(s). This signal has an integrated pull-down resistor.
AC_SDOUT	O	**AC97 Serial Data Out:** Serial TDM data output to the Codec(s). **NOTE:** AC_SDOUT is sampled at the rising edge of PWROK as a functional strap.
AC_SDIN[1:0]	I	**AC97 Serial Data In 2:**0: These signals are Serial TDM data inputs from the three Codecs.

NOTE: An integrated pull-down resistor on AC_BIT_CLK is enabled when either: The ACLINK Shutoff bit in the AC'97 Global Control Register is set to 1, or Both Function 5 and Function 6 of Device 31 are disabled. Otherwise, the integrated pull-down resistor is disabled.

General Purpose I/O Signals

Signal Name	Type	Description
GPIO[43:32]	I/O	Can be input or output. Main power well.
GPIO[31:29]	O	Not implemented.
GPIO[28:27]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[26]	I/O	Not implemented.
GPIO[25]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[24:18]	I/O	Not Implemented in Mobile (Assign to native Functionality).
GPIO[17:16]	O	Fixed as Output only. Main power well. Can be used instead as PC/PCI GNT[A:B]#. GPIO[17] can also alternatively be used for PCI GNT[5]#. Integrated pull-up resistor.
GPIO[15:14]	I	Not implemented.
GPIO[13:12]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[11]	I	Fixed as Input only. Resume power well. Can be used instead as SMBALERT#.
GPIO[10:9]	I	Not implemented.
GPIO[8]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[7]	I	Fixed as Input only. Main power well. Unmuxed.
GPIO[6]	I	Not Implemented in Mobile (Assign to Native Functionality)
GPIO[5:2]	I	Fixed as Input only. Main power well. Can be used instead as PIRQ[E:H]#.
GPIO[1:0]	I	Fixed as Input only. Main power well. Can be used instead as PC/PCI REQ[A:B]#. GPIO[1] can also alternatively be used for PCI REQ[5]#.

NOTE: Main power well GPIO are 5V tolerant, except for GPIO[43:32]. Resume power well GPIO are not 5V tolerant.

Power and Ground Signals

Signal Name	Description
VCC3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VCC1_5	1.5 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
VCCHI	1.5 V supply for Hub Interface 1.5 logic. 1.8 V supply for Hub Interface 1.0 logic. This power may be shut off in S3, S4, S5 or G3 states.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
HIREF	Analog Input. Expected voltages are: • 0.9 V for HI 1.0 (Normal Hub Interface) Series Termination • 350 mV for HI 1.5 (Enhanced Hub Interface) Parallel Termination This power is shut off in S3, S4, S5, and G3 states.
VCCSUS3_3	3.3 V supply for resume well I/O buffers. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCSUS1_5	1.5 V supply for resume well logic. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
V5REF_SUS	Reference for 5 V tolerance on resume well inputs. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCLAN3_3	3.3 V supply for LAN Connect interface buffers. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCLAN1_5	1.5 V supply for LAN Controller logic. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. **NOTE:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap.
VCCPLL	1.5 V supply for core well logic. This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states.
VBIAS	RTC well bias voltage. The DC reference voltage applied to this pin sets a current that is mirrored throughout the oscillator and buffer circuitry.
V_CPU_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface outputs.
VSS	Grounds.

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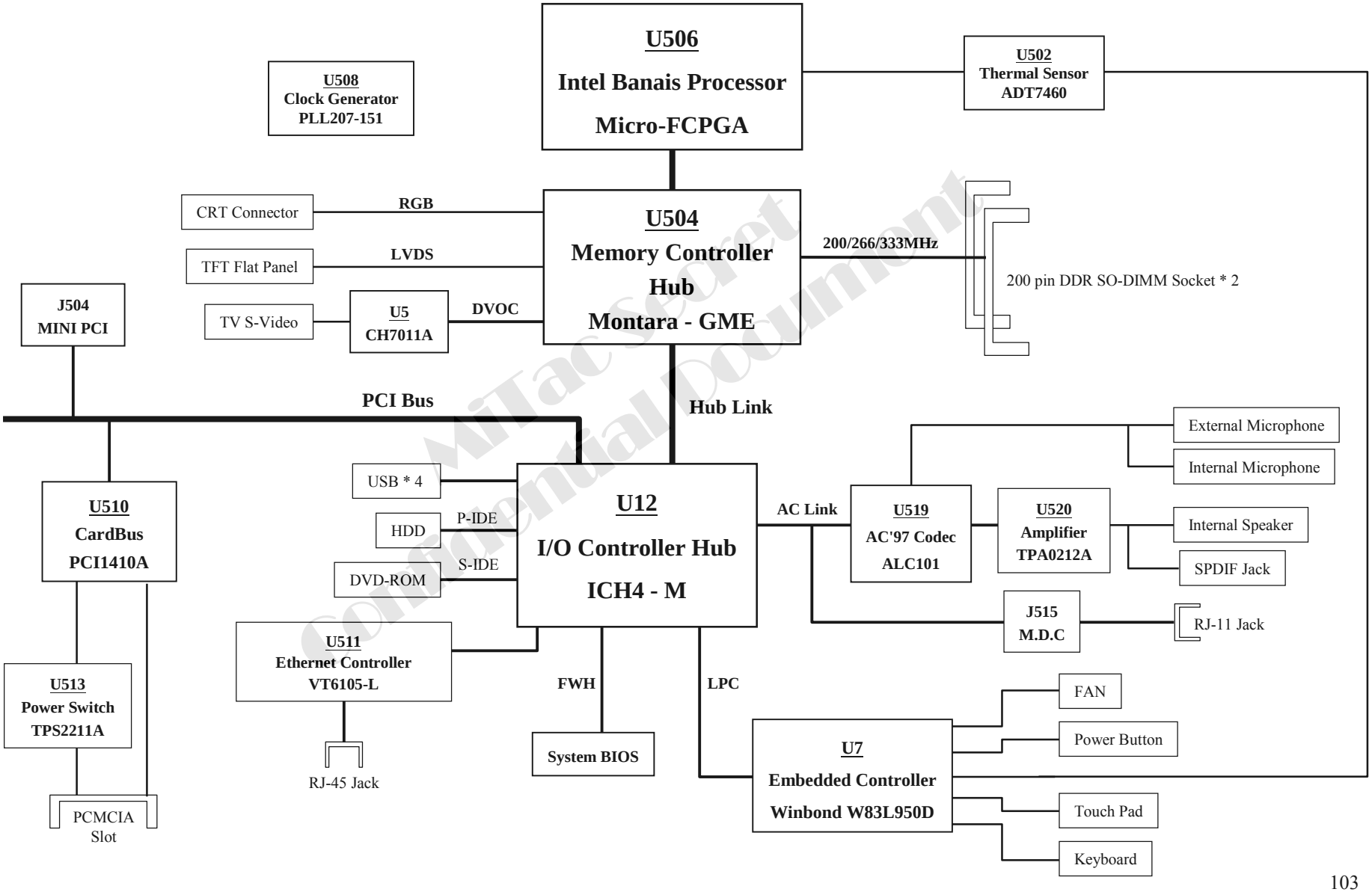
6. System Block Diagram



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7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port by the debug card plug at MINI PCI slot.

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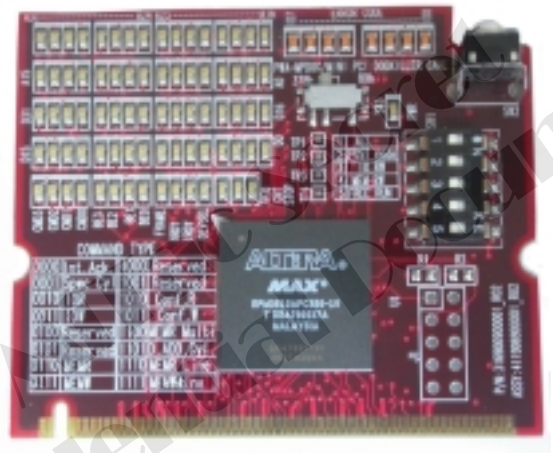
7.2 Maintenance Diagnostics

7.2.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA; PWA-MPDOG/MINI PCI DOGKILLER CARD
Note: Order it from MIC/TSSC

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7.3 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign on messages displayed

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7.3 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville
52h	USB HC init

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8. Trouble Shooting

- 8.1 No Power
- 8.2 No Display
- 8.3 VGA Controller Failure LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.7 Hard Driver Test Error
- 8.8 CD-ROM Driver Test Error
- 8.9 USB Port Test Error
- 8.10 Audio Failure
- 8.11 LAN Test Error
- 8.12 PC Card Socket Failure
- 8.13 TV Test Error

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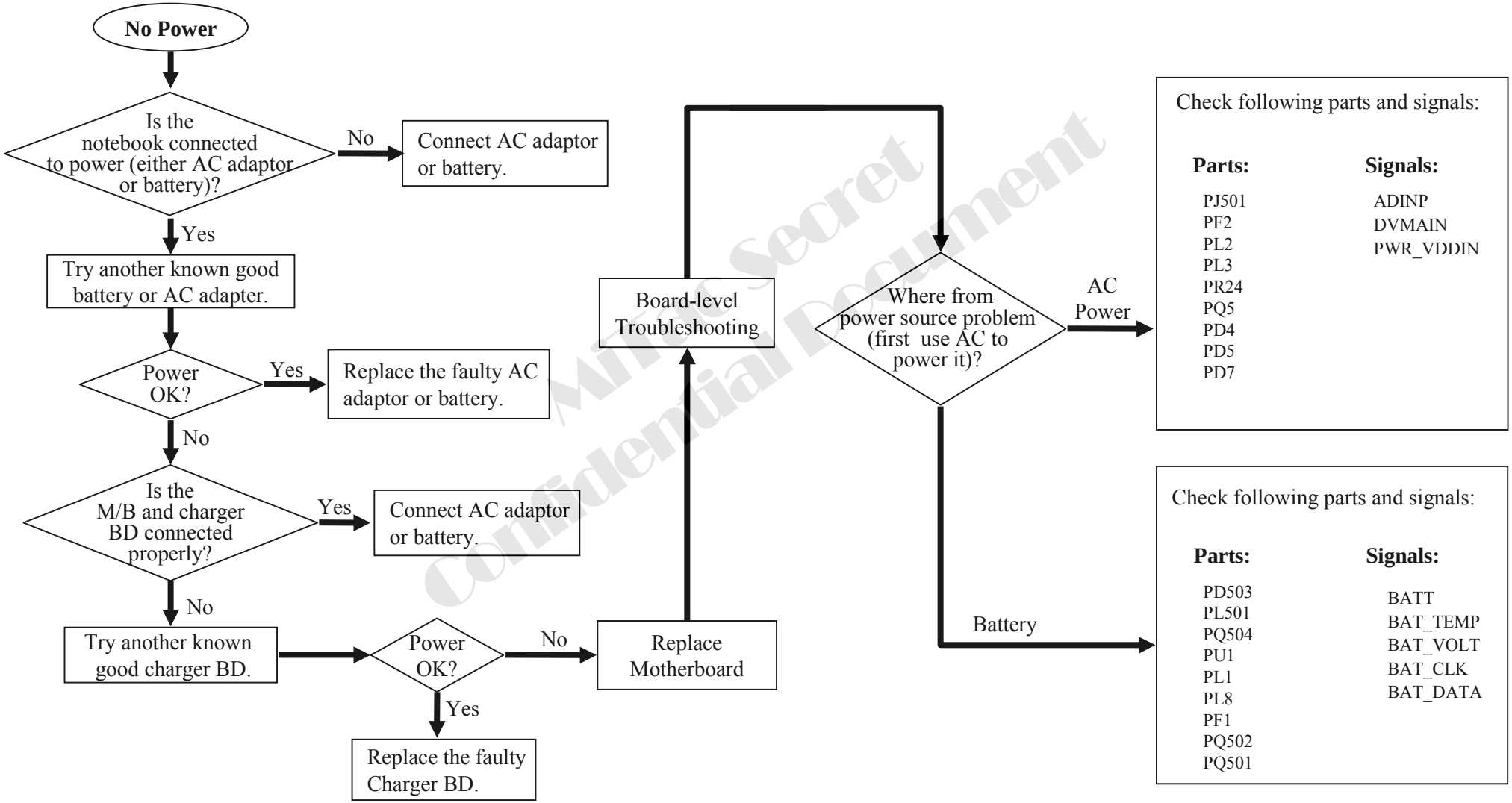
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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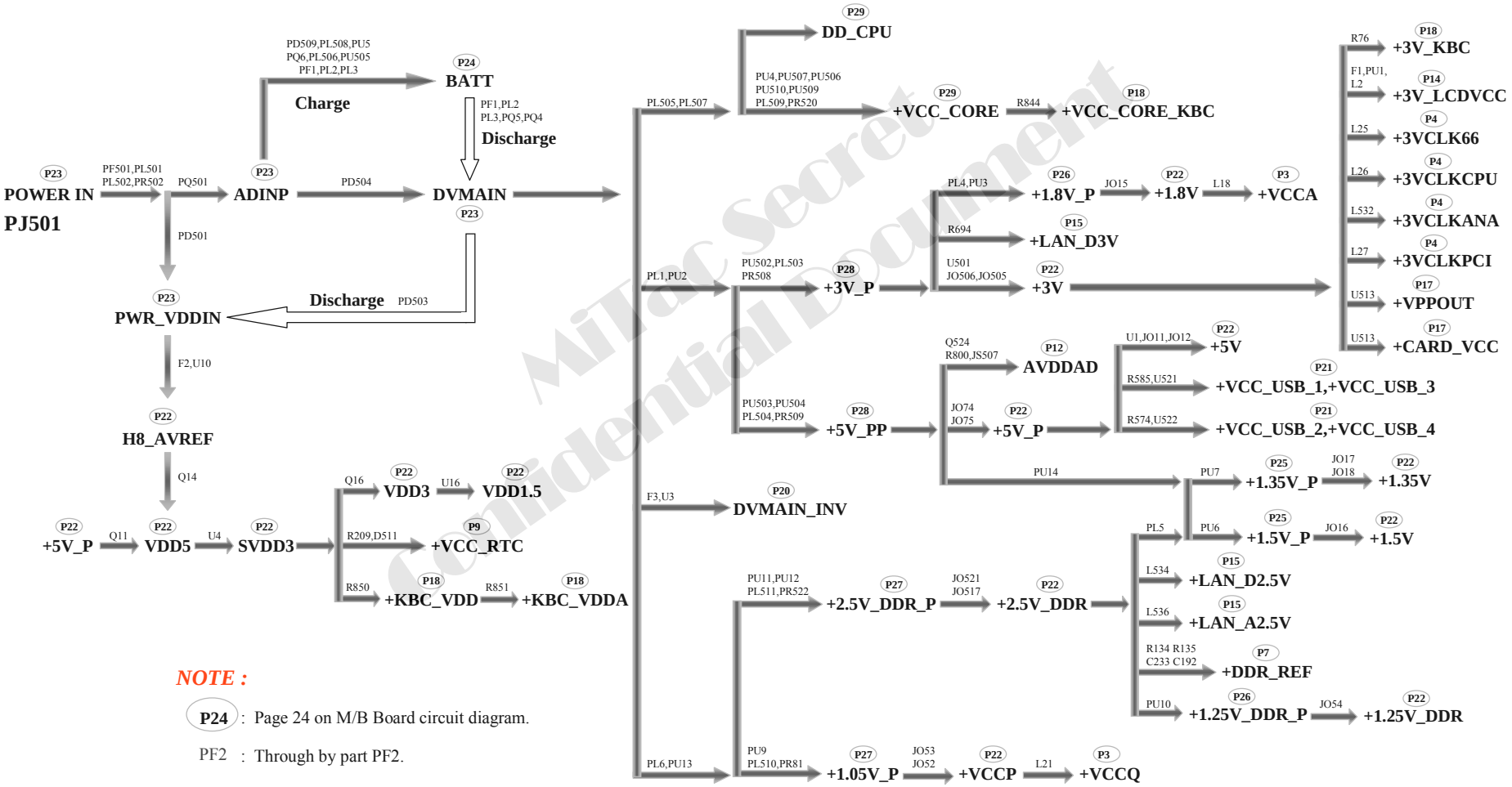
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



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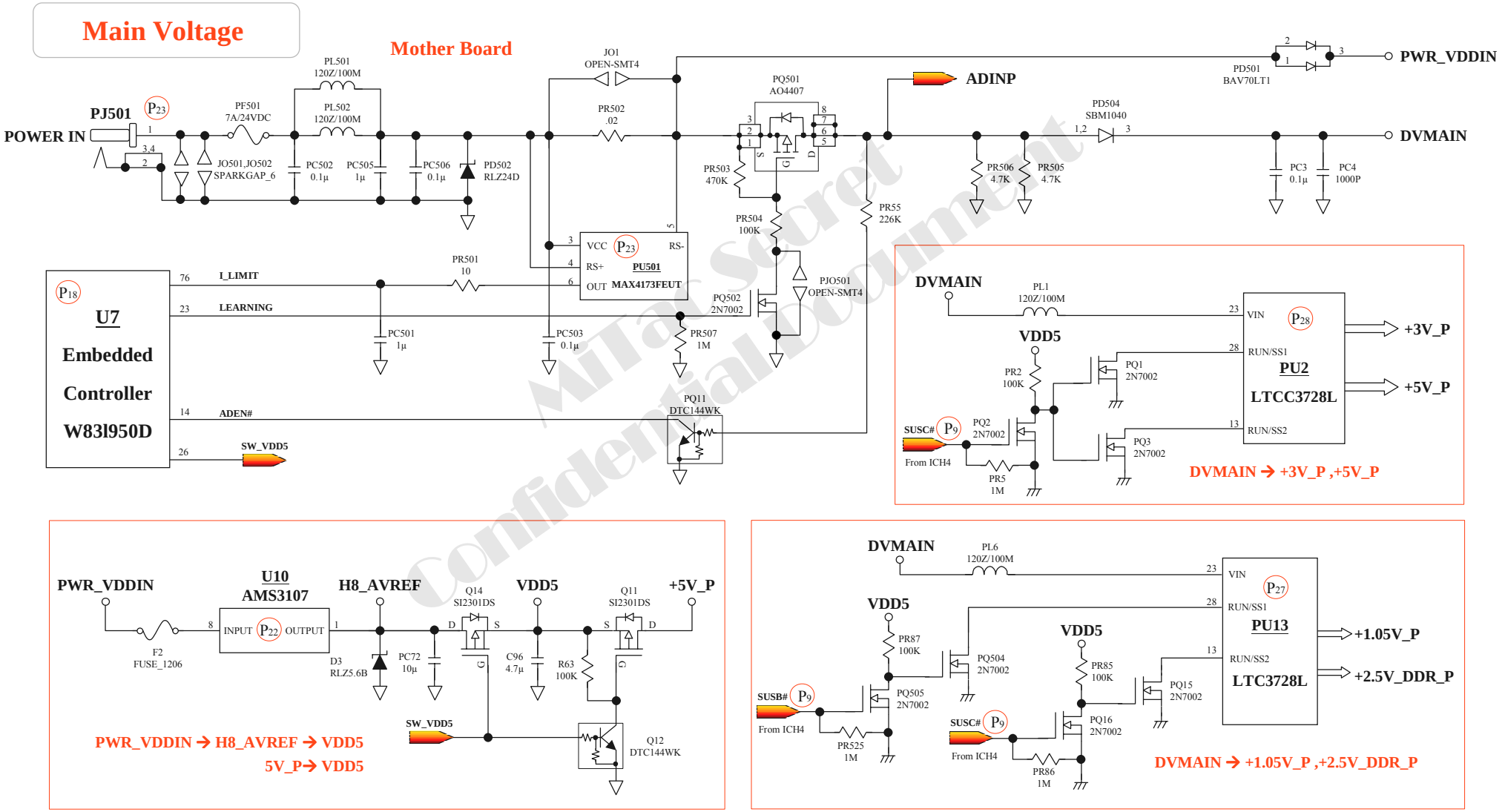
NOTE :

P24 : Page 24 on M/B Board circuit diagram.

PF2 : Through by part PF2.

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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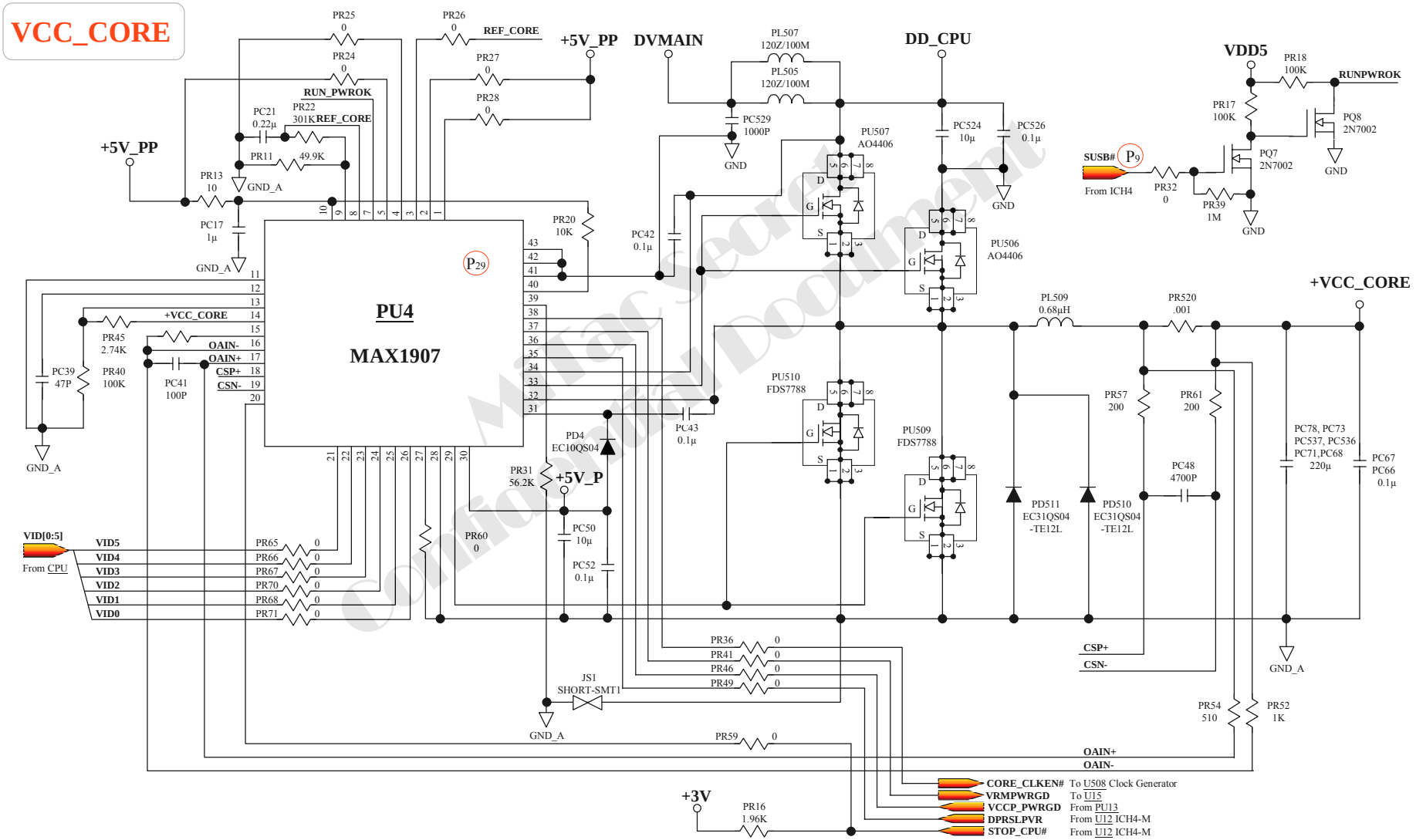
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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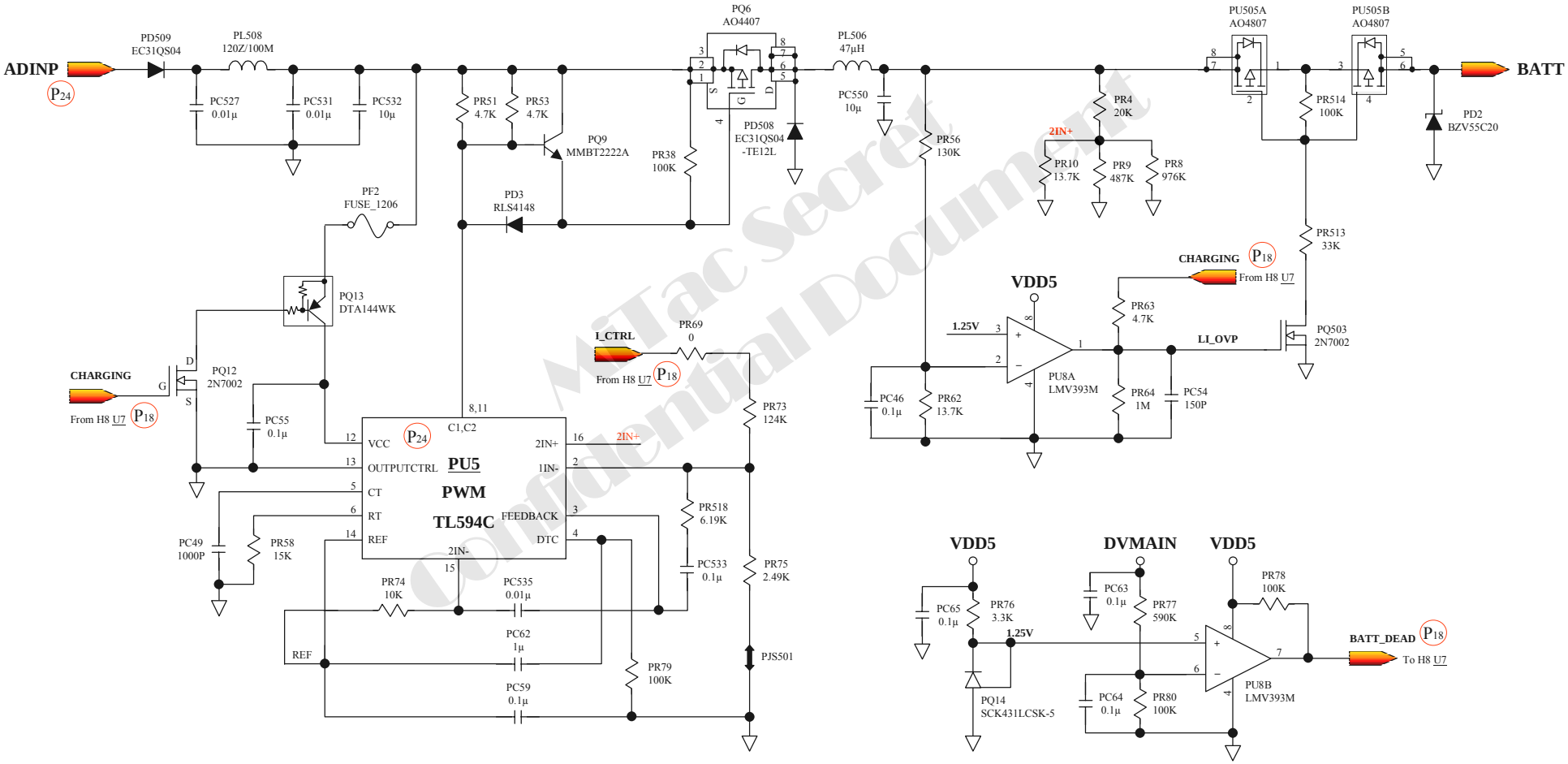
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Charge



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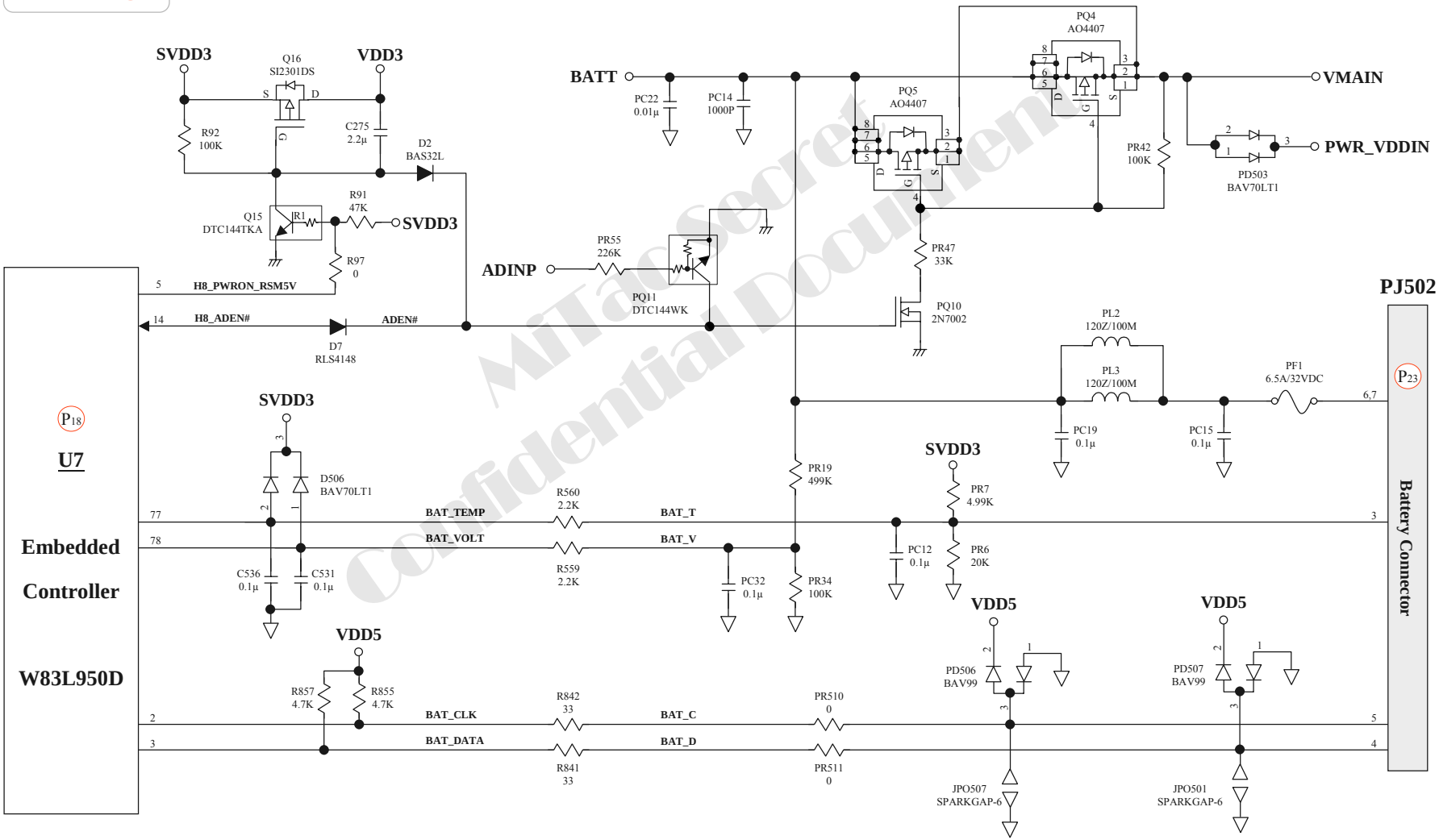
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Discharge



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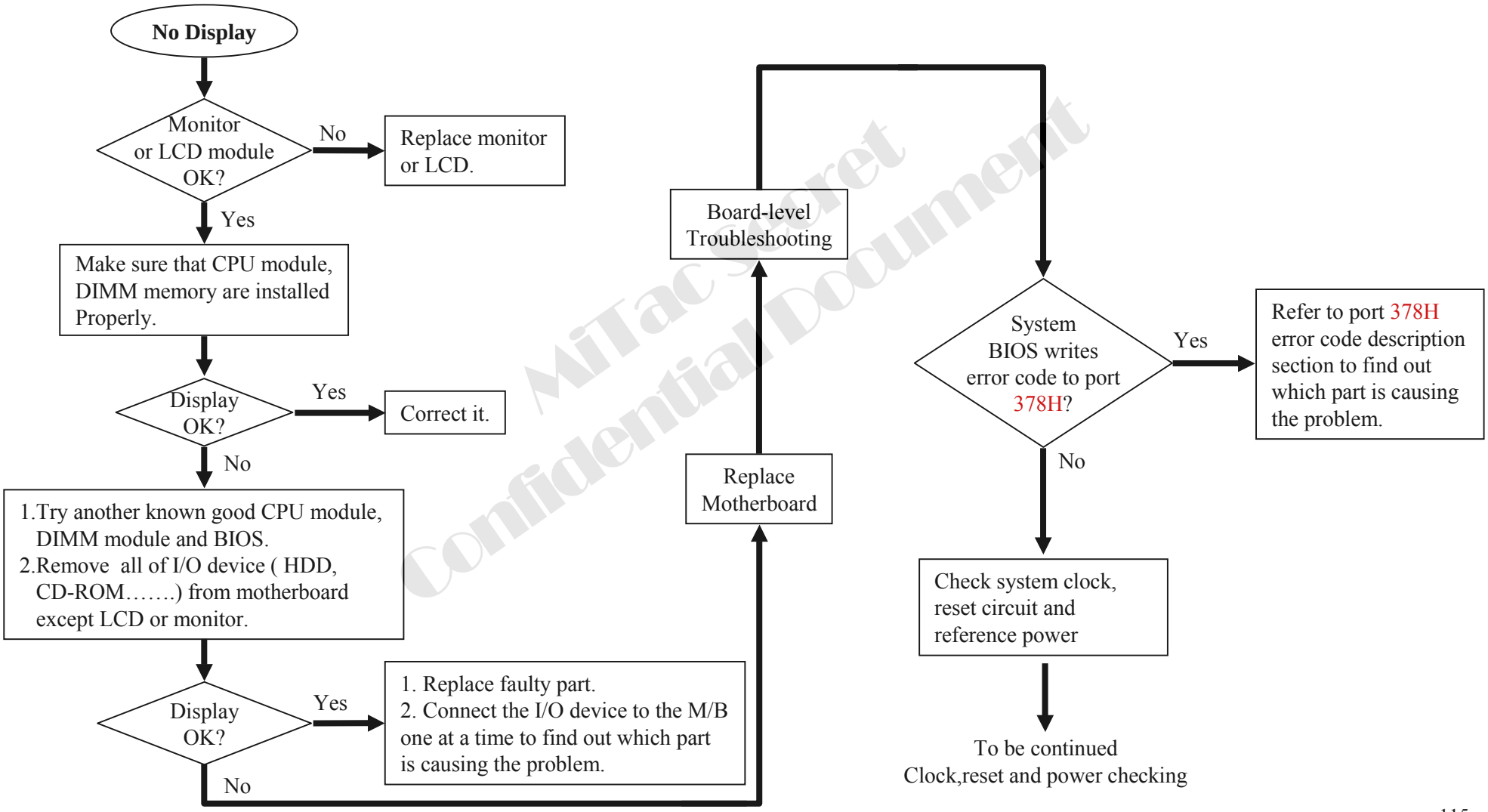
8.2 No Display

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.


No Display
Monitor or LCD module OK?
No
Replace monitor or LCD.
Yes
Make sure that CPU module, DIMM memory are installed Properly.
Display OK?
Yes
Correct it.
No
1.Try another known good CPU module, DIMM module and BIOS.
2.Remove all of I/O device (HDD, CD-ROM…….) from motherboard except LCD or monitor.
Display OK?
Yes
1. Replace faulty part.
2. Connect the I/O device to the M/B one at a time to find out which part is causing the problem.
No
Replace Motherboard
Board-level Troubleshooting
System BIOS writes error code to port 378H?
Yes
Refer to port 378H error code description section to find out which part is causing the problem.
No
Check system clock, reset circuit and reference power
To be continued
Clock,reset and power checking

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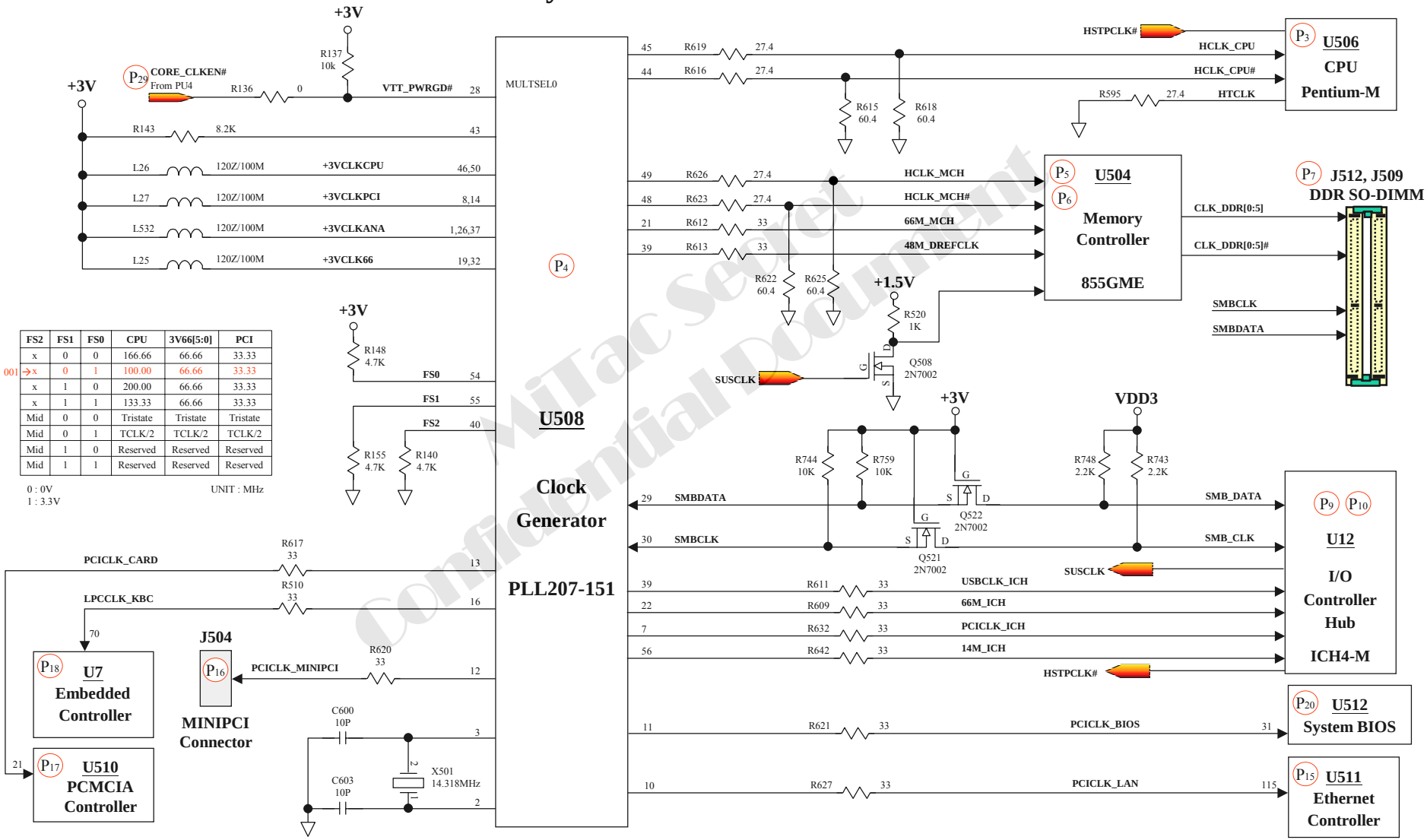
8.2 No Display

****** System Clock Check ******



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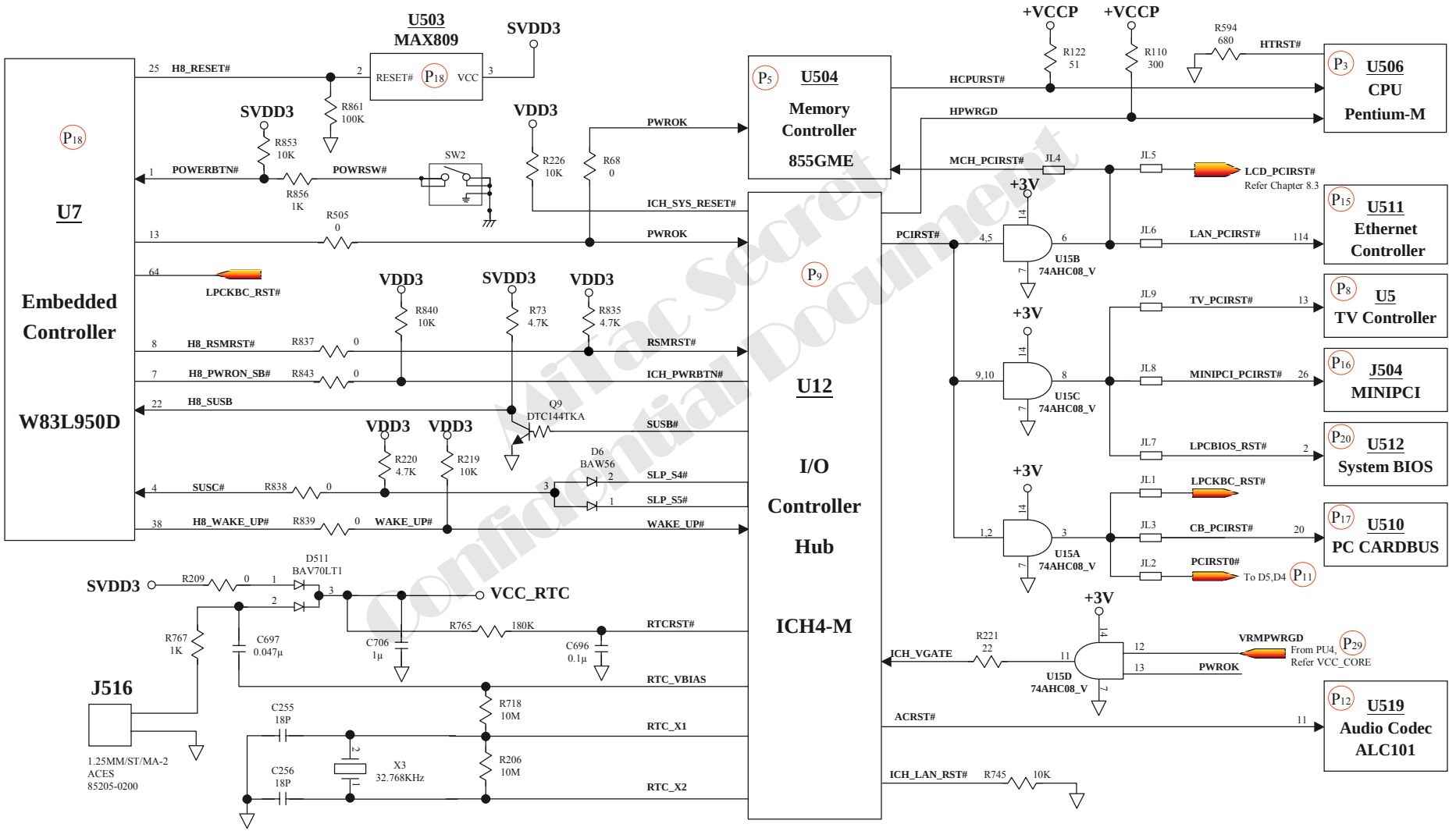
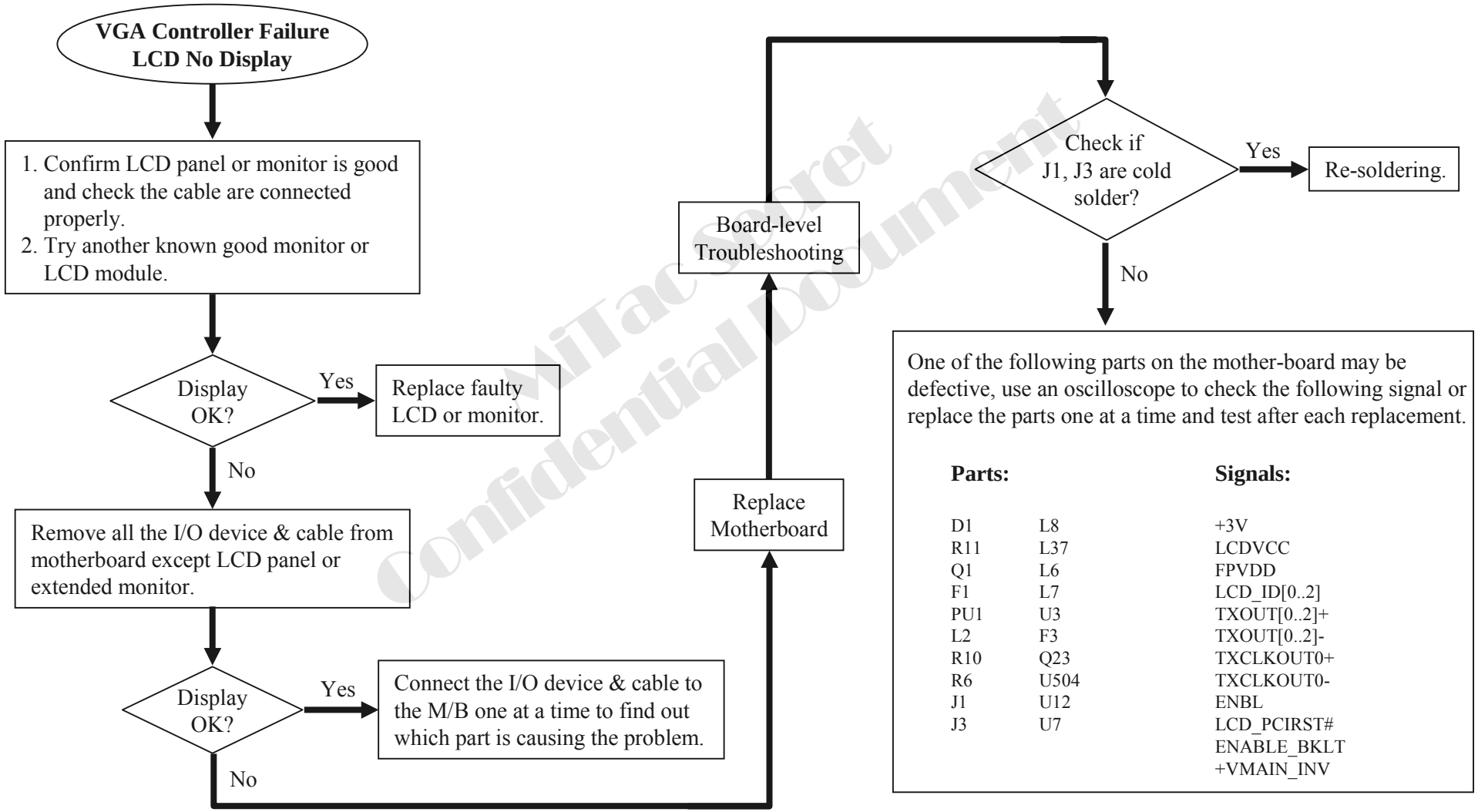
8.2 No Display

****** Power Good & Reset Circuit Check ******



8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



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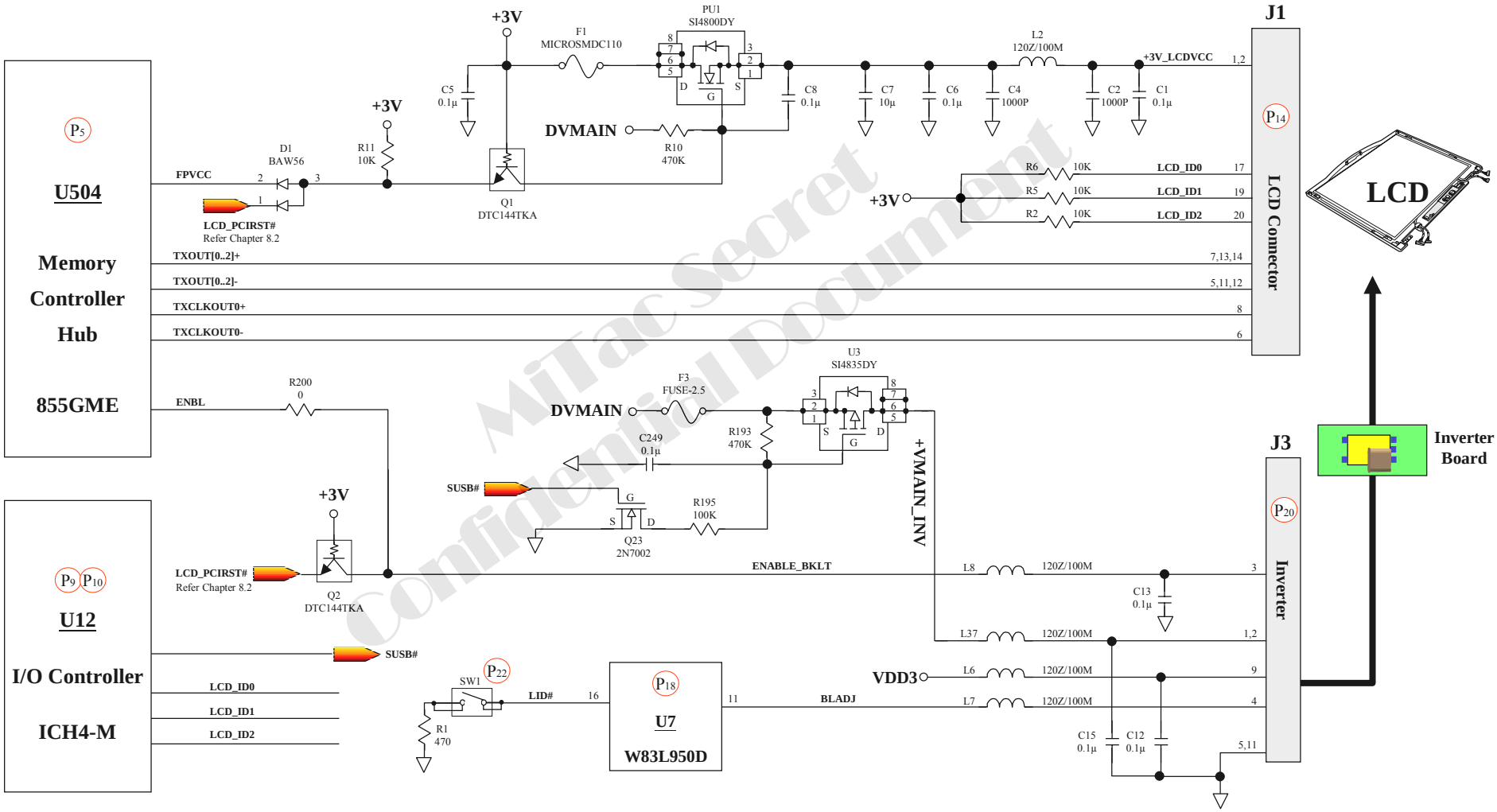
8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



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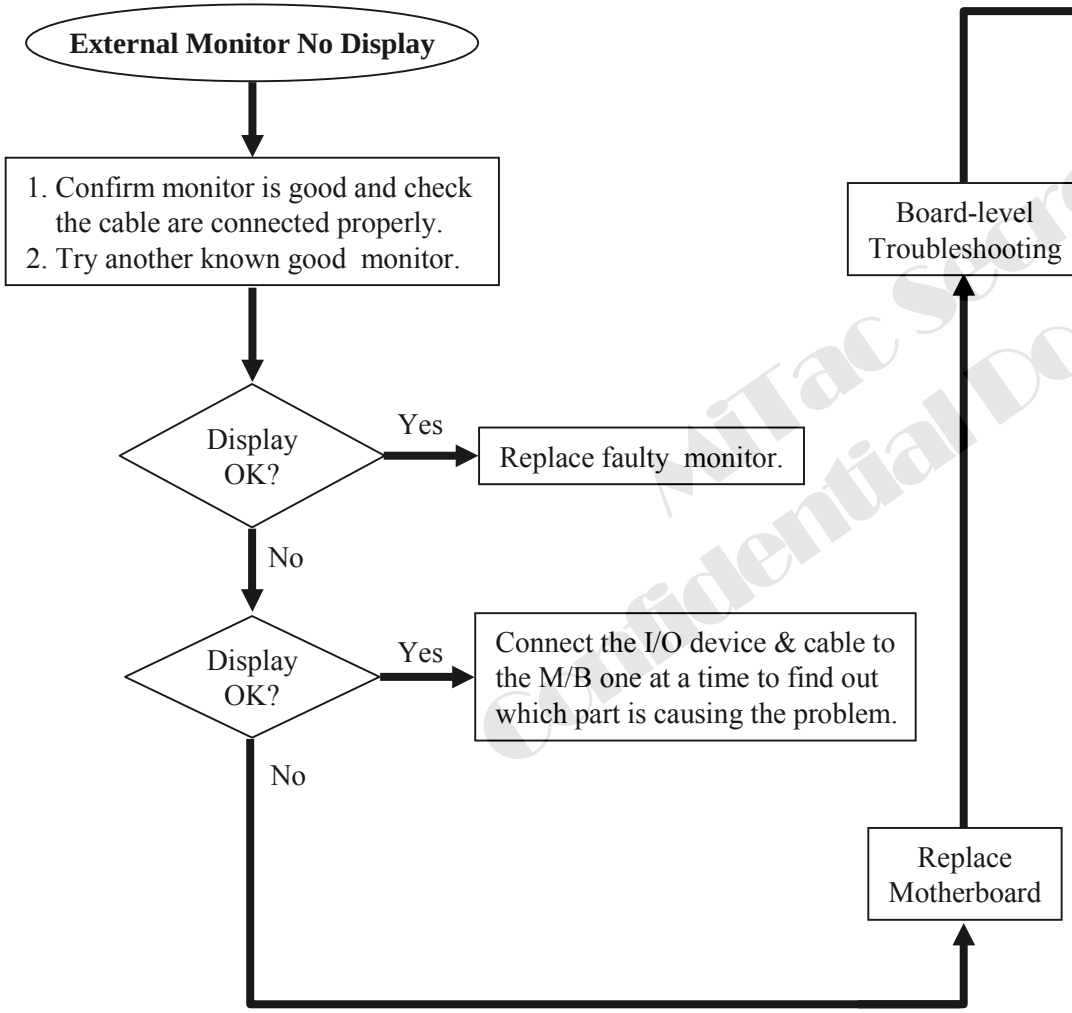
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



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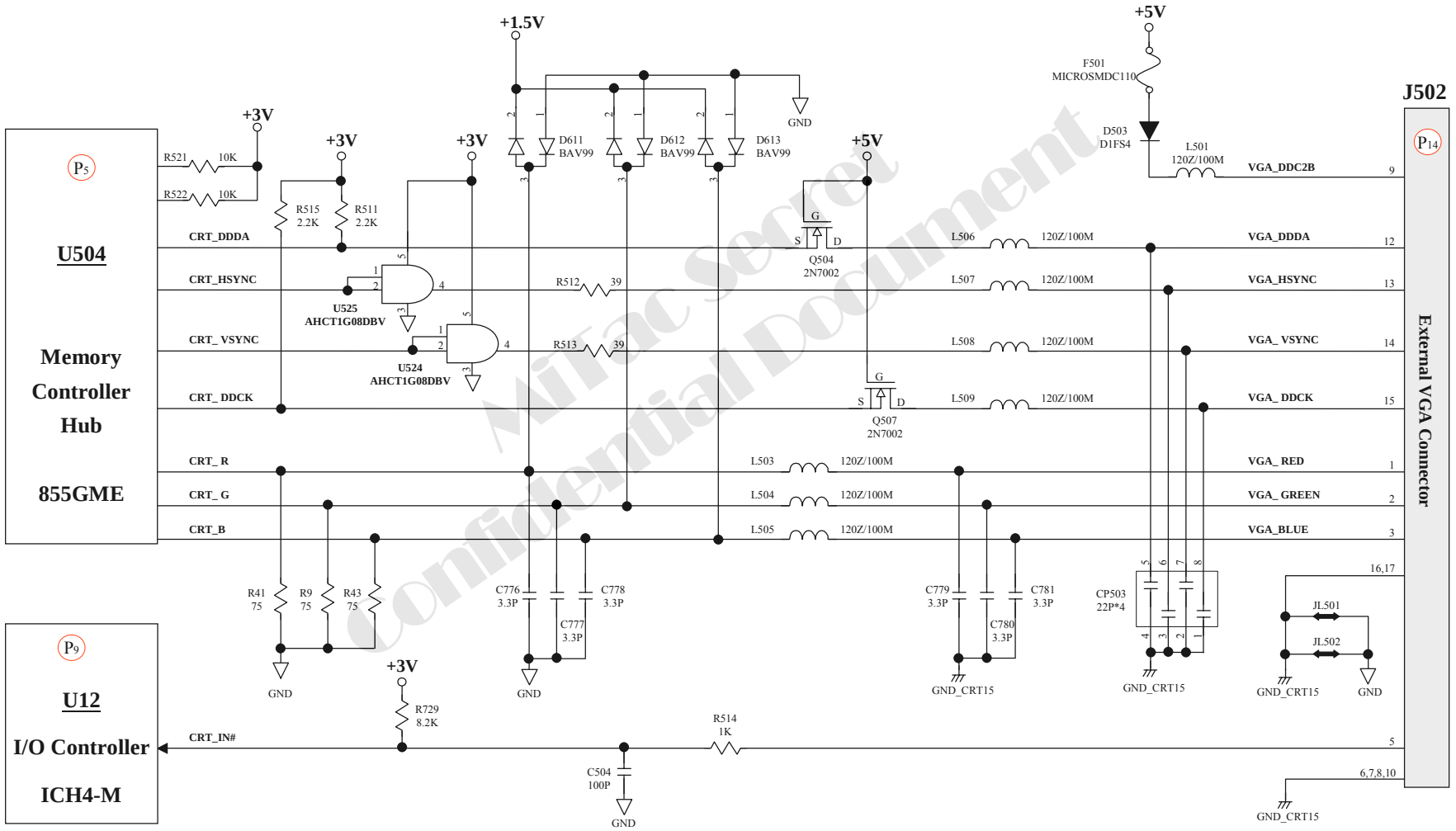
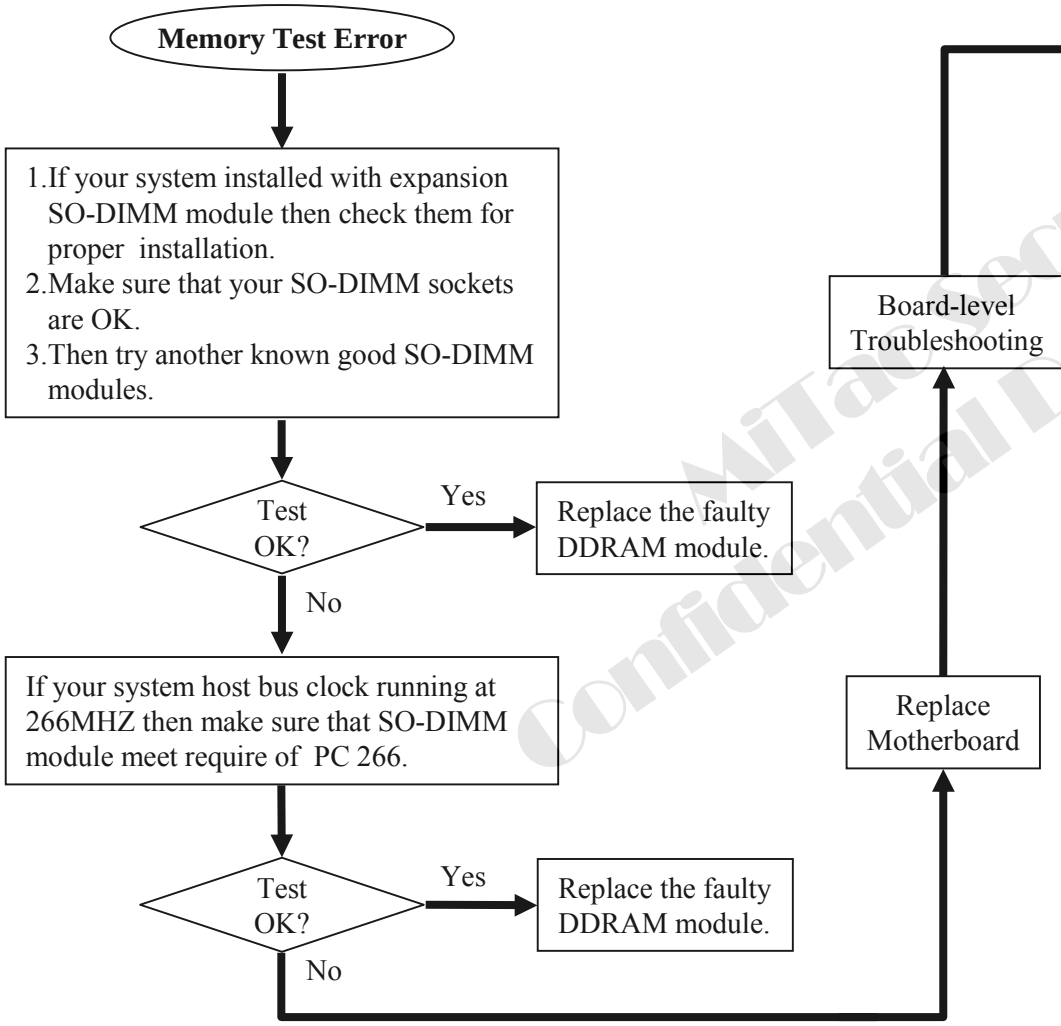
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8.5 Memory Test Error

Extend DDRAM is failure or system hangs up.


Memory Test Error
1.If your system installed with expansion SO-DIMM module then check them for proper installation.
2.Make sure that your SO-DIMM sockets are OK.
3.Then try another known good SO-DIMM modules.
Test OK?
Yes
Replace the faulty DDRAM module.
No
If your system host bus clock running at 266MHZ then make sure that SO-DIMM module meet require of PC 266.
Test OK?
Yes
Replace the faulty DDRAM module.
No
Replace Motherboard
Board-level Troubleshooting

One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

Parts:

RP1~RP13
RP13~RP29
R78
R130
Q521
Q522
J512
J509
U504
U12
U508
R743
R748

Signals:

+1.25V_DDR
+2.5V_DDR
CKE [0..3],
CS# [0..3]
SMA [1,2,4,5]
SMAB [1,2,4,5]
NB_MA [0,3,6..12]
NB_MD [0..63]
NB_DQS [0..8],
NB_BA [0,1]
NB_CB [0..7],
NB_DM [0..8]
NB_RAS#
NB_CAS#
NB_WE#
SMB_DATA
SMB_CLK
HCLK_MCH
HCLK_MCH#
66M_MCH
CLK_DDR [0..5]
CLK_DDR [0..5]#

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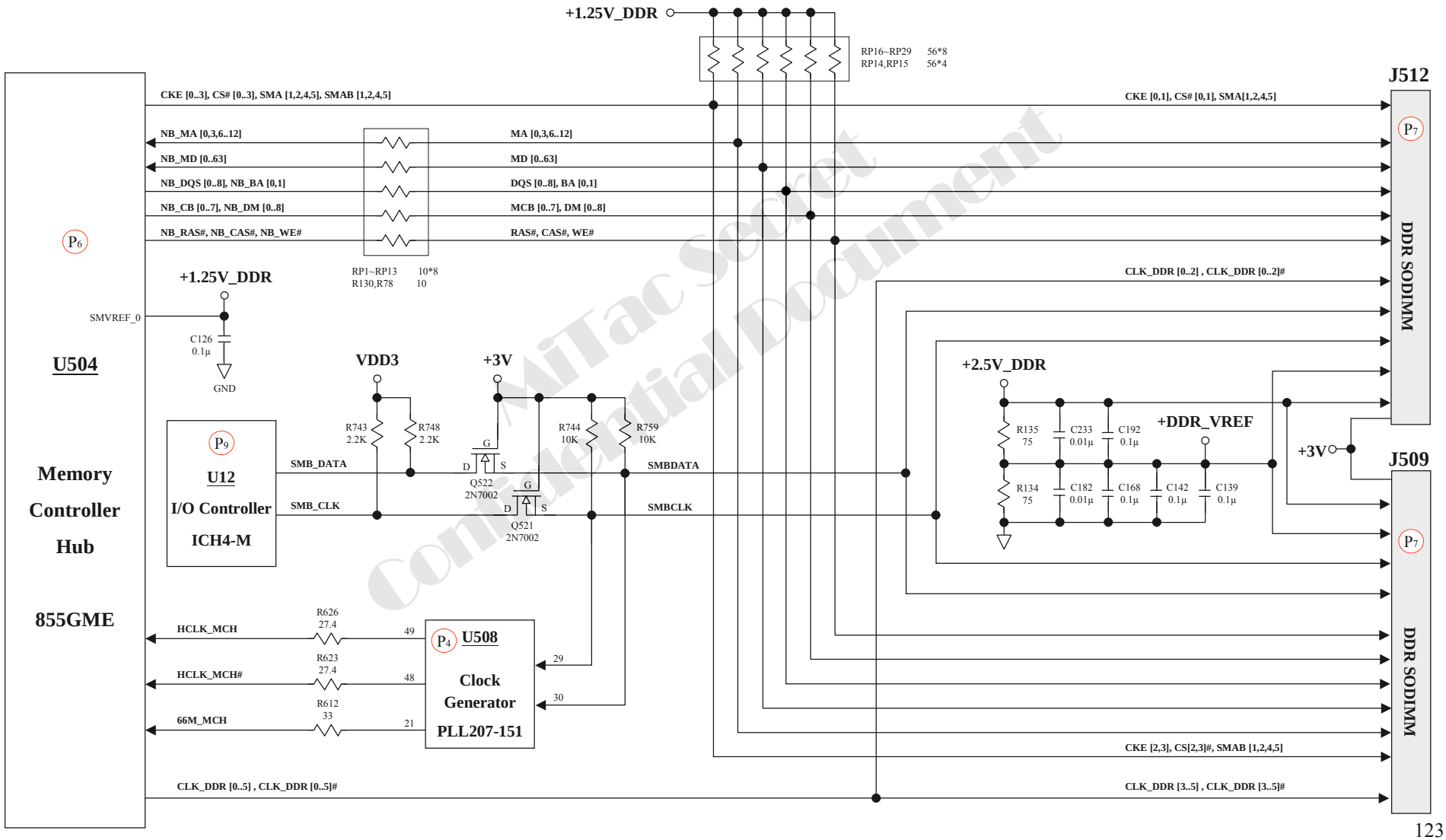
8.5 Memory Test Error

Extend DDRAM is failure or system hangs up.



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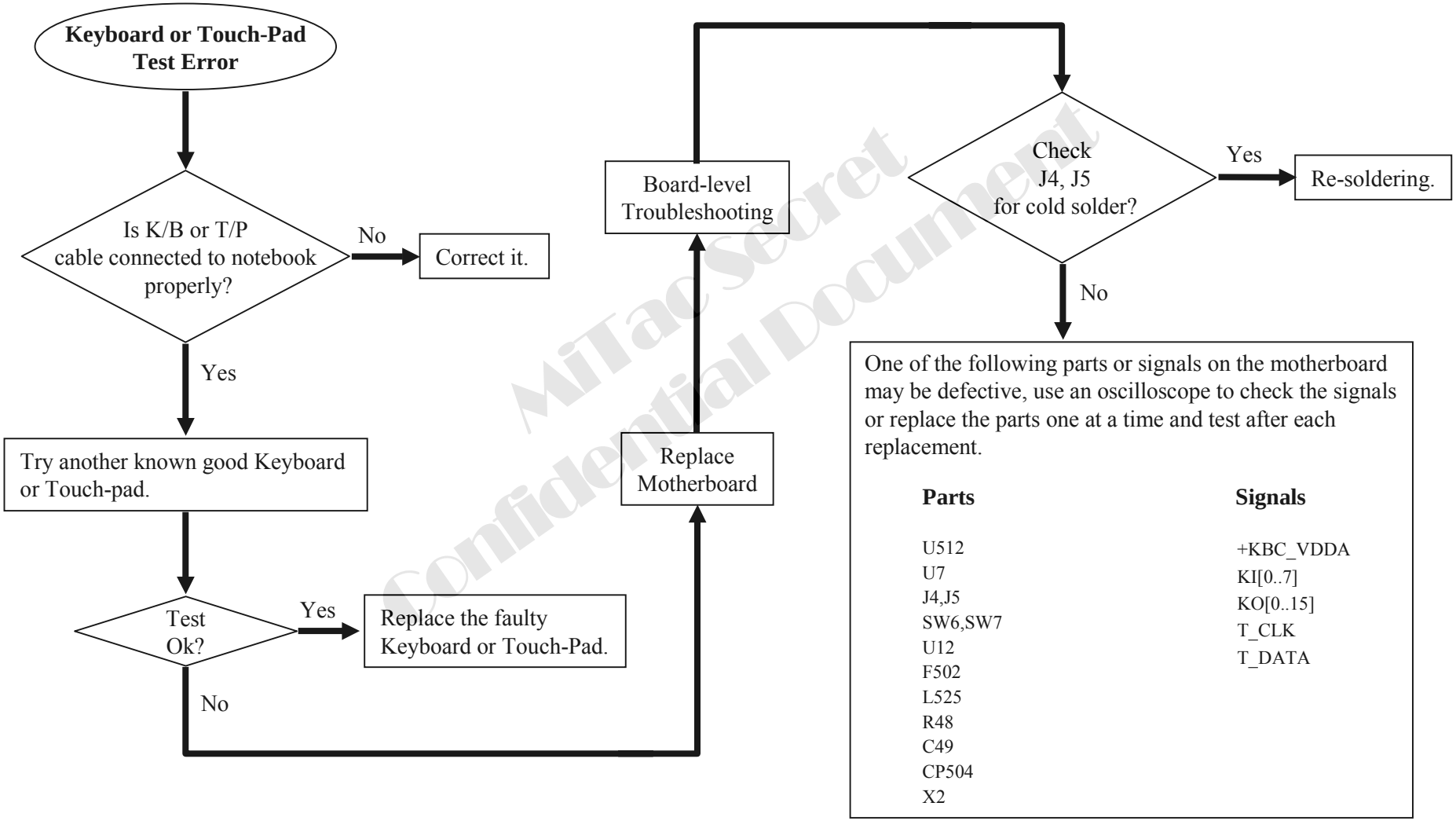
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



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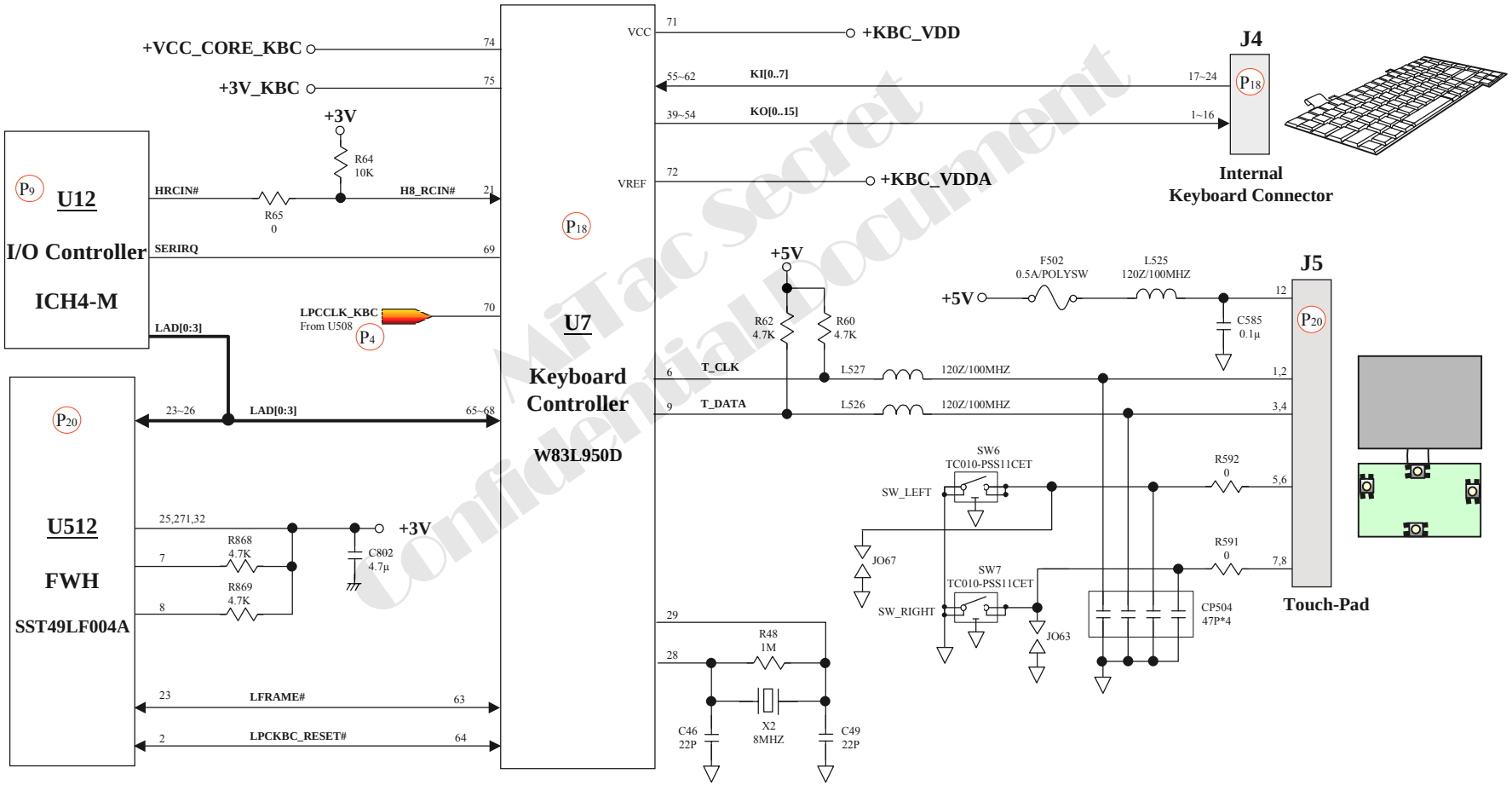
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



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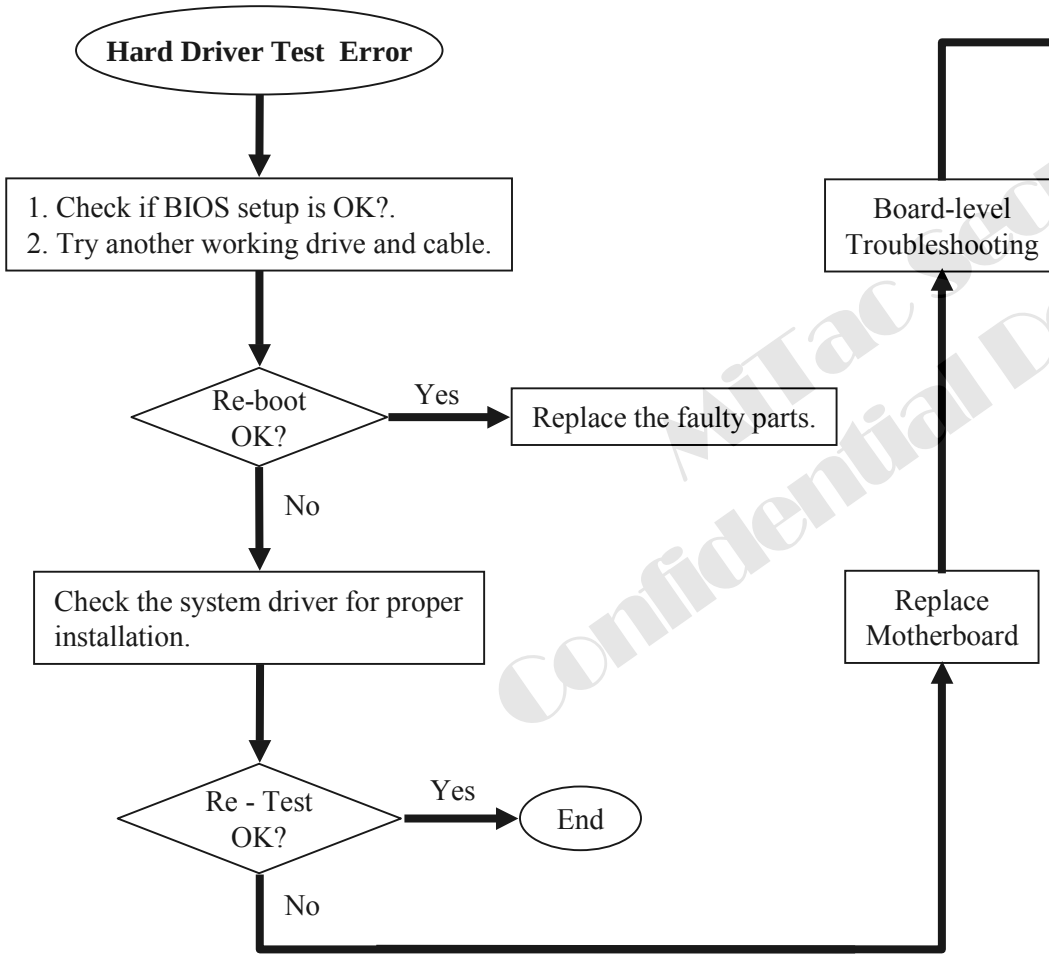
8.7 Hard Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U12	+5V
J514	HDD_LED#
Q19	PD_D[0..15]
D5	IDERST#
R187	PDCS1#
L49	PDA[0..2]
R196	PDDACK#
	PIORDY
	PDIOR#
	PDIOW#
	PDREQ
	PDCS3#
	IRQ14

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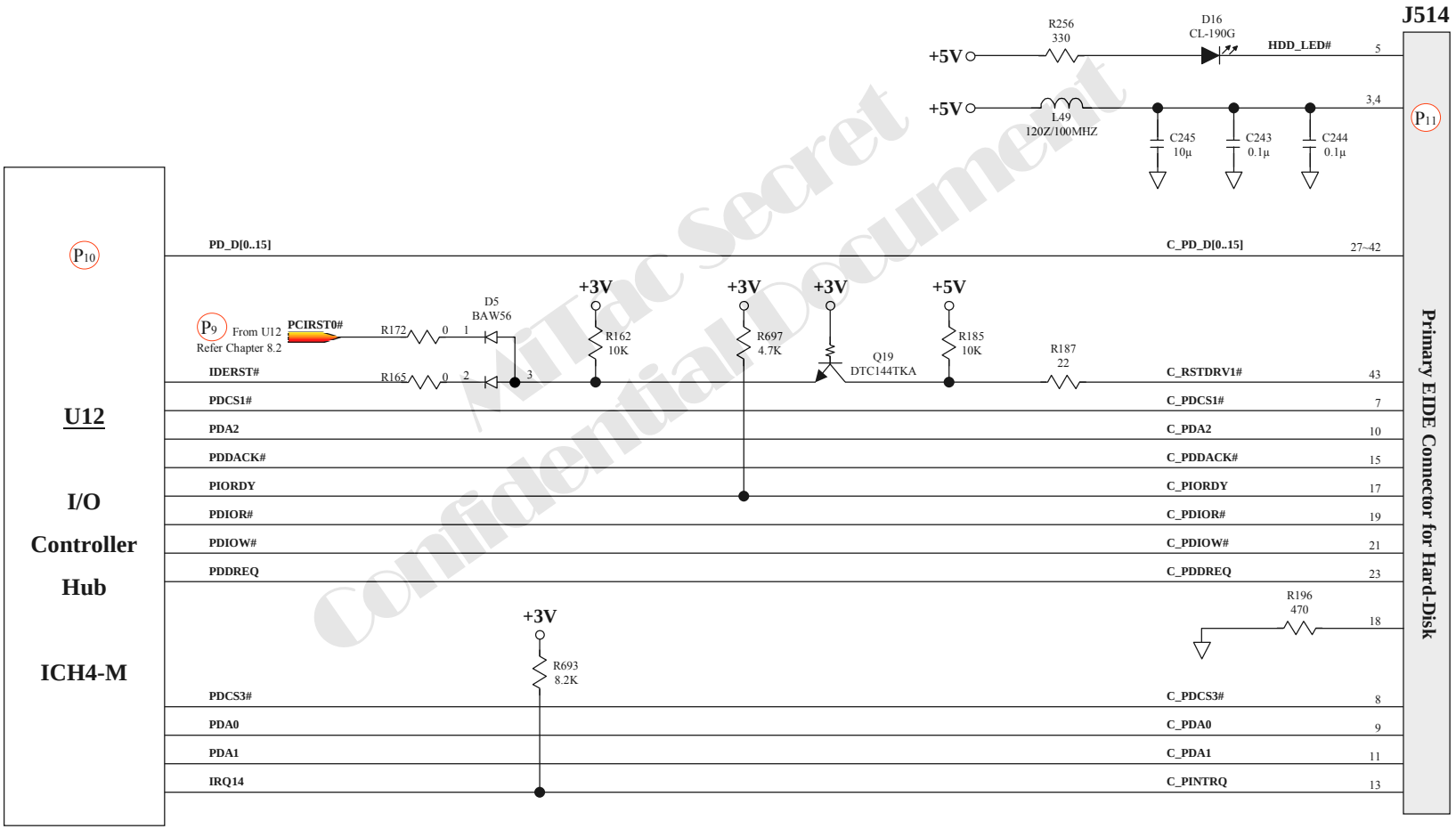
8.7 Hard Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



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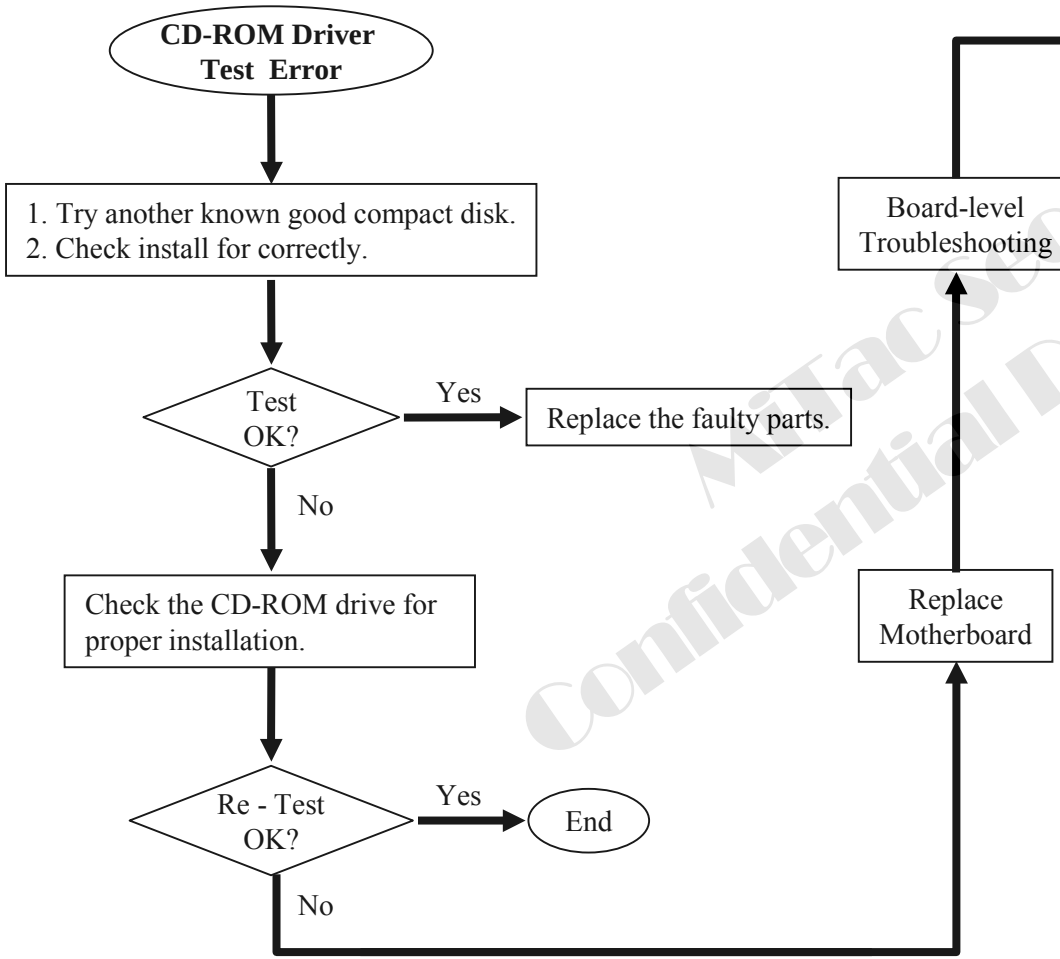
8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U12	+5V
J510	CD_LED#
Q18	SD_D[0..15]
D4	SIDERST#
R183	SDA[0..2]
R655	IRQ15
R673	SDDACK#
R164	SIORDY
L50	SDIOW#
C141	SDDREQ
	SDIOR#
	SDCS1#
	SDCS3#

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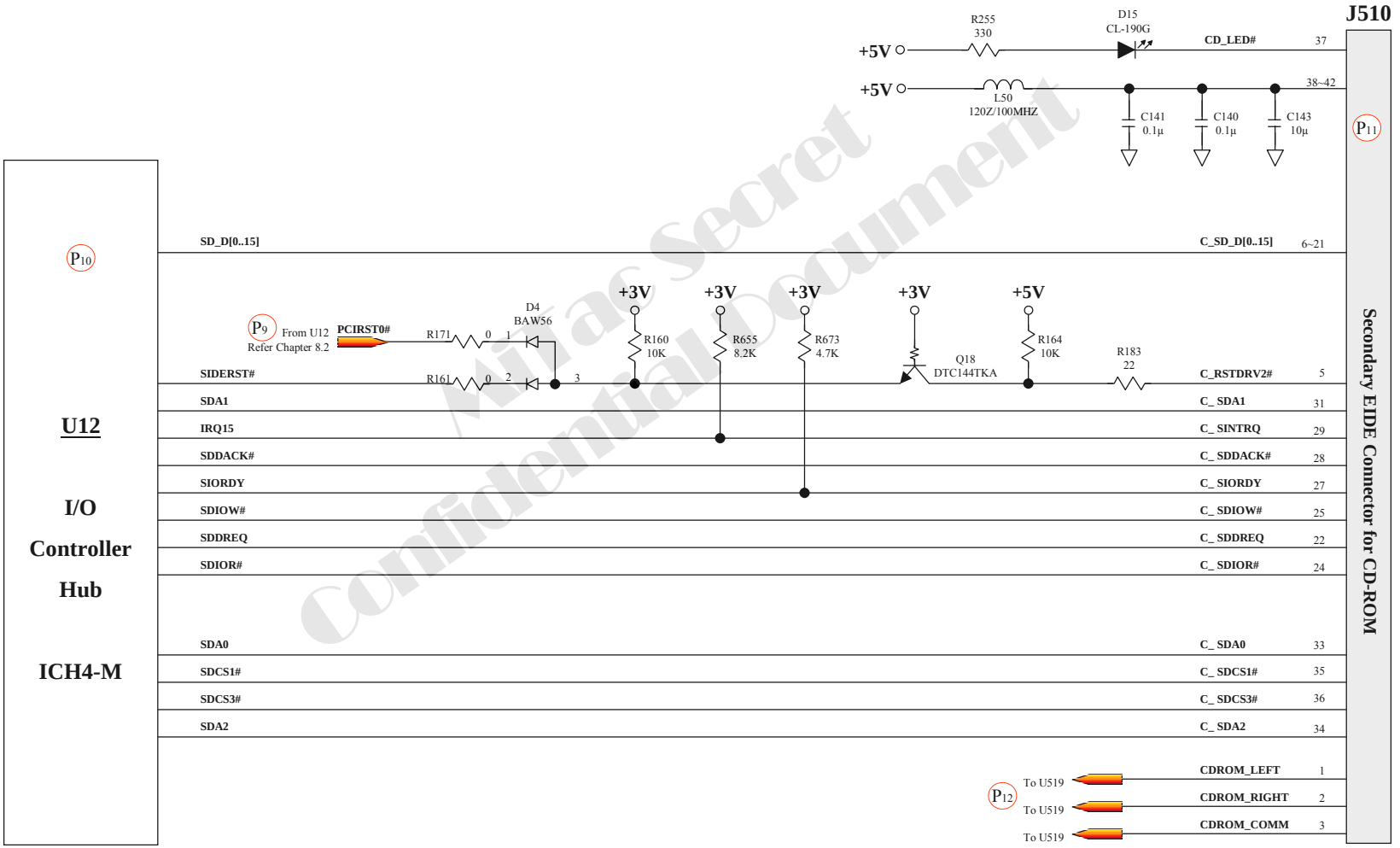
8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



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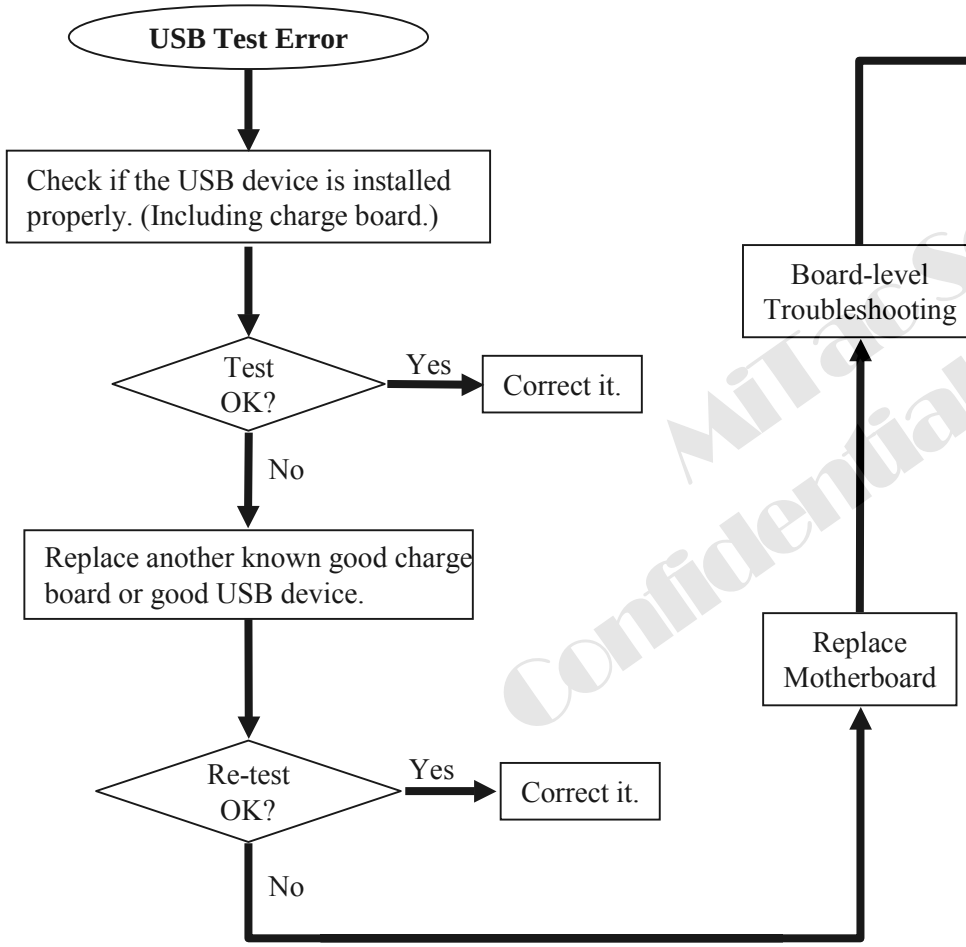
8.9 USB Test Error

An error occurs when a USB I/O device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U12	+5V_P
J507	USBOC1#
J506	USBOC3#
U521	USBP[0..3]+
U522	USBP[0..3]-
L44	
L47	
L38	
L41	
R585	
R574	
C763	

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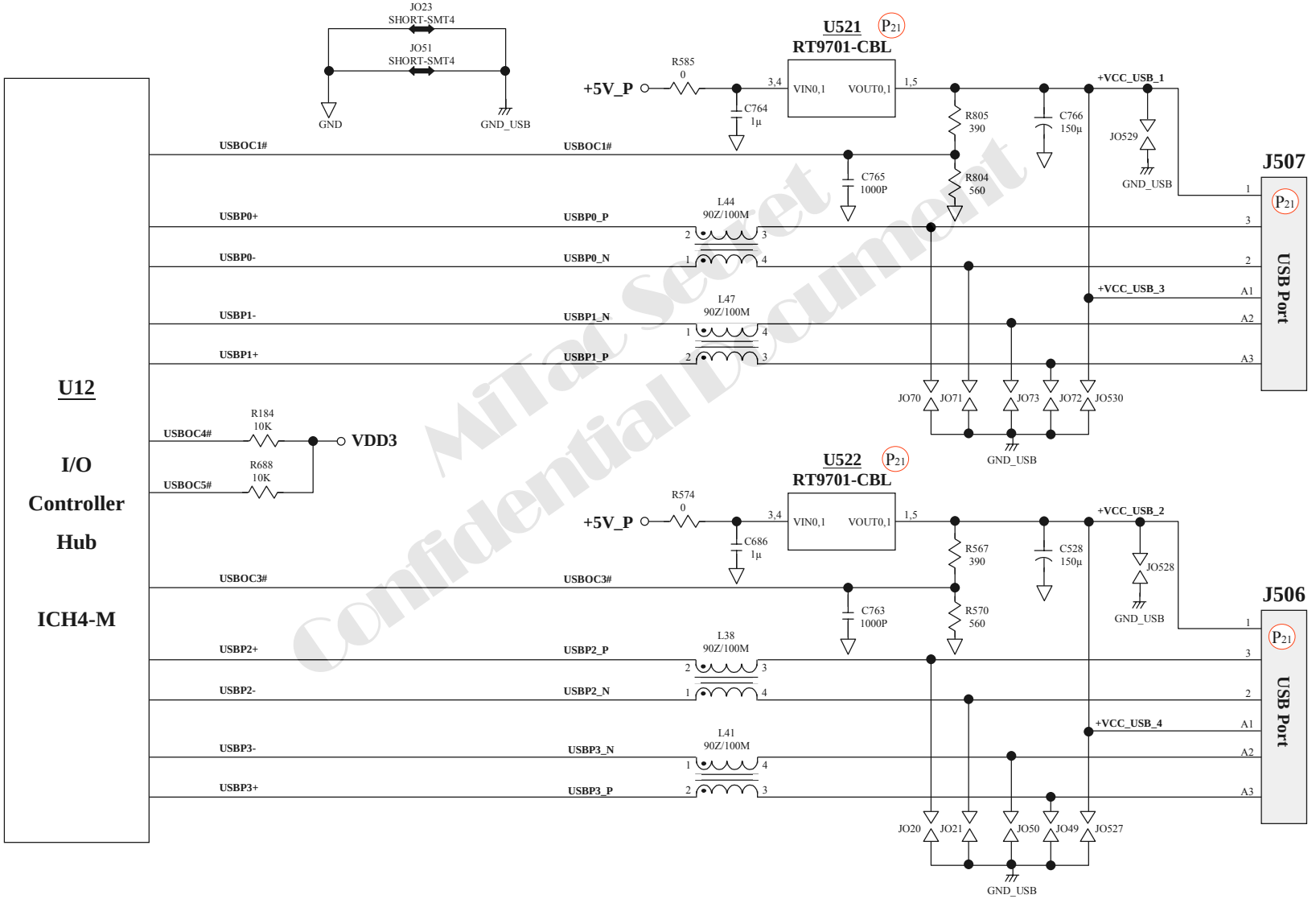
8.9 USB Test Error

An error occurs when a USB I/O device is installed.



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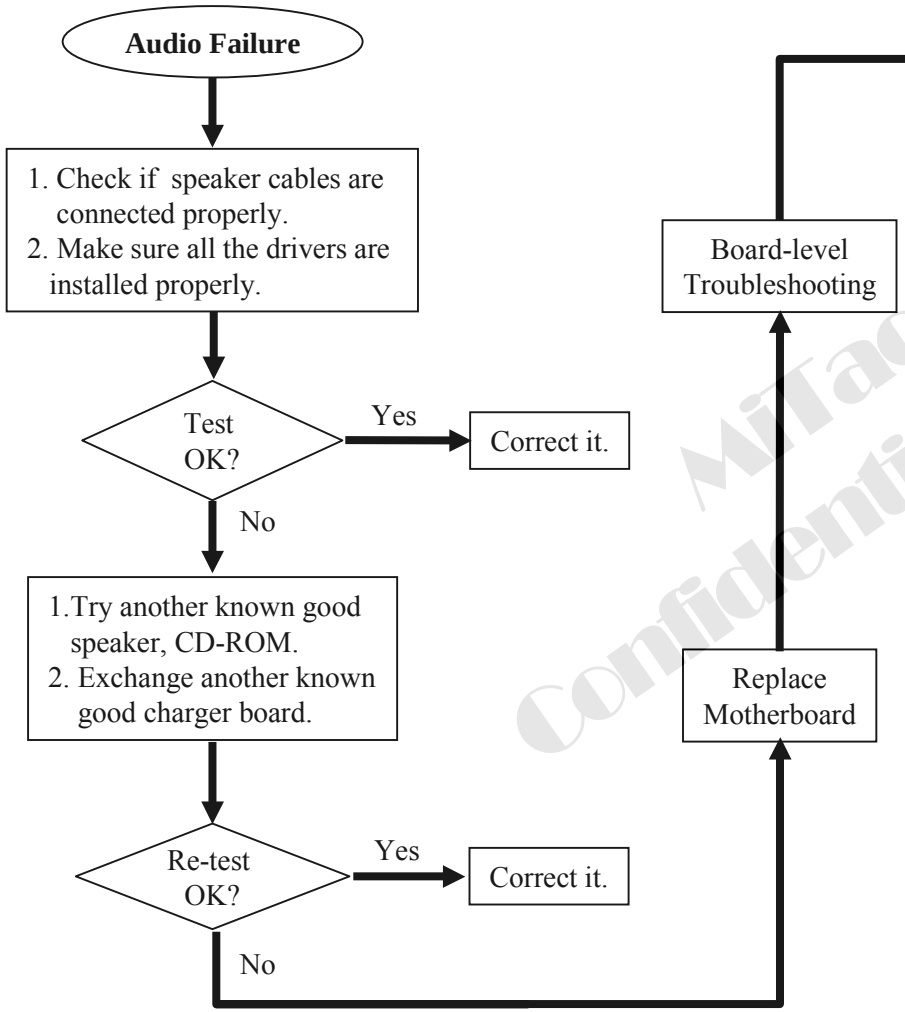
8.10 Audio Failure

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U12	AOUT_R
U510	AOUT_L
U519	ACRST#
U18	ACSDOUT
J9	ACSDIN0
J2	ACSDYNC
J503	ACBITCLK
R785	+3V
C735	AVDDAD
R779	SPK_OFF
C723	
R243	
L34	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U12	H8_AVREF
U510	MIC
J8	
L33	
L546	
R506	
R238	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U519	CDROM_LEFT
J510	CDROM_RIGHT
R242	CDROM_COMM
R240	
C745	
C743	

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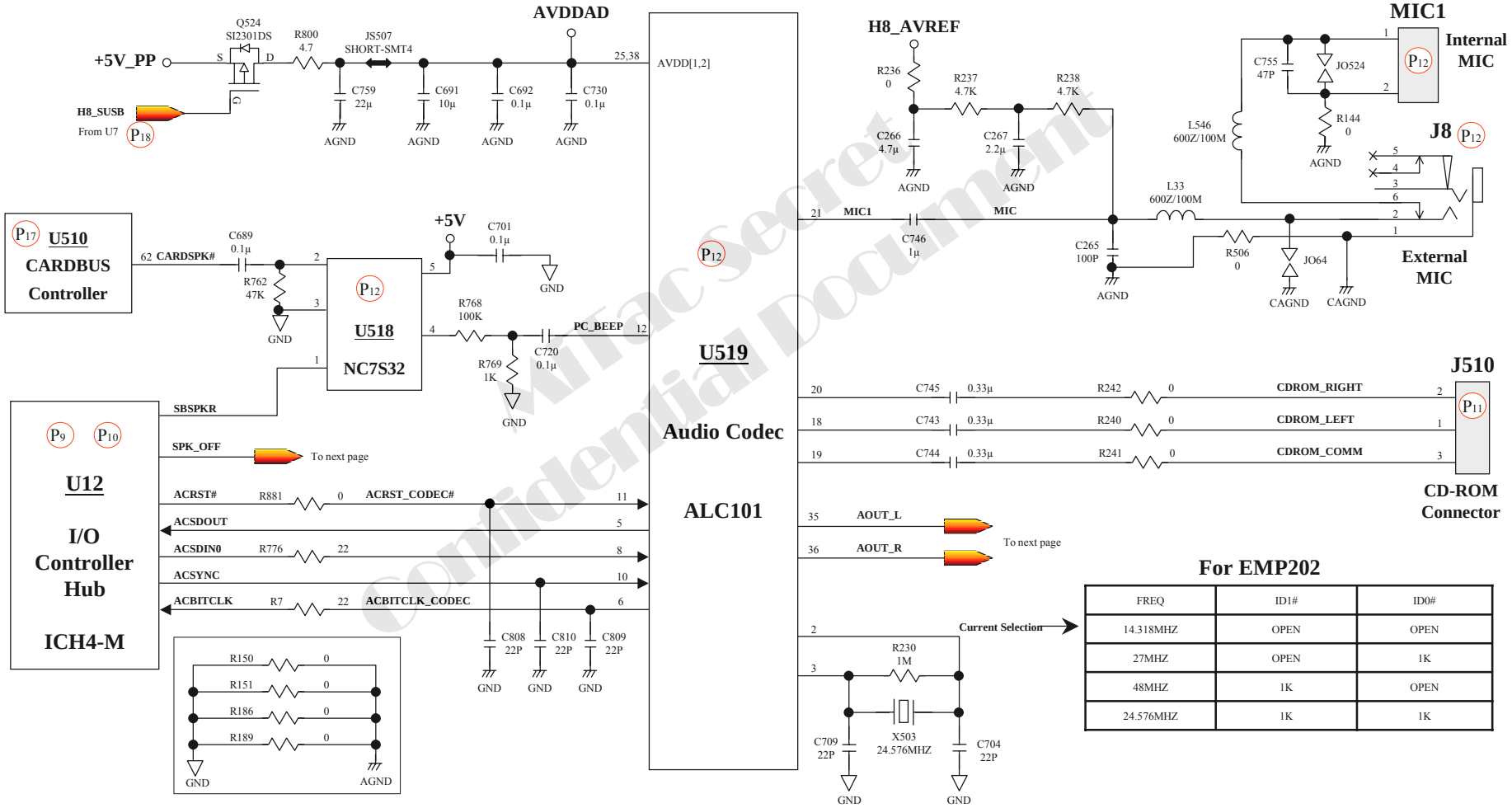
8.10 Audio Failure – Audio IN

No sound from speaker after audio driver is installed.



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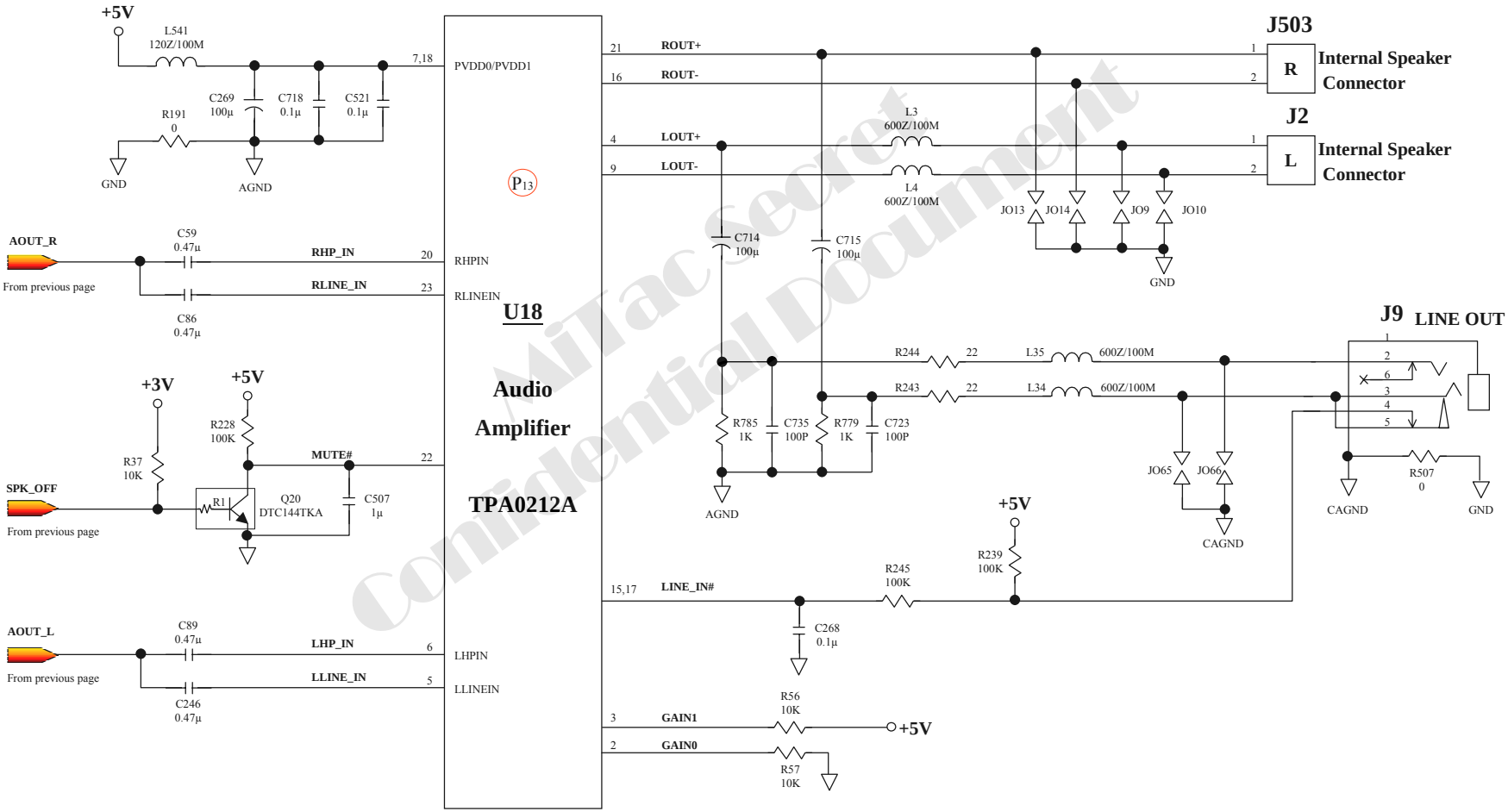
8.10 Audio Failure – Audio OUT

No sound from speaker after audio driver is installed.



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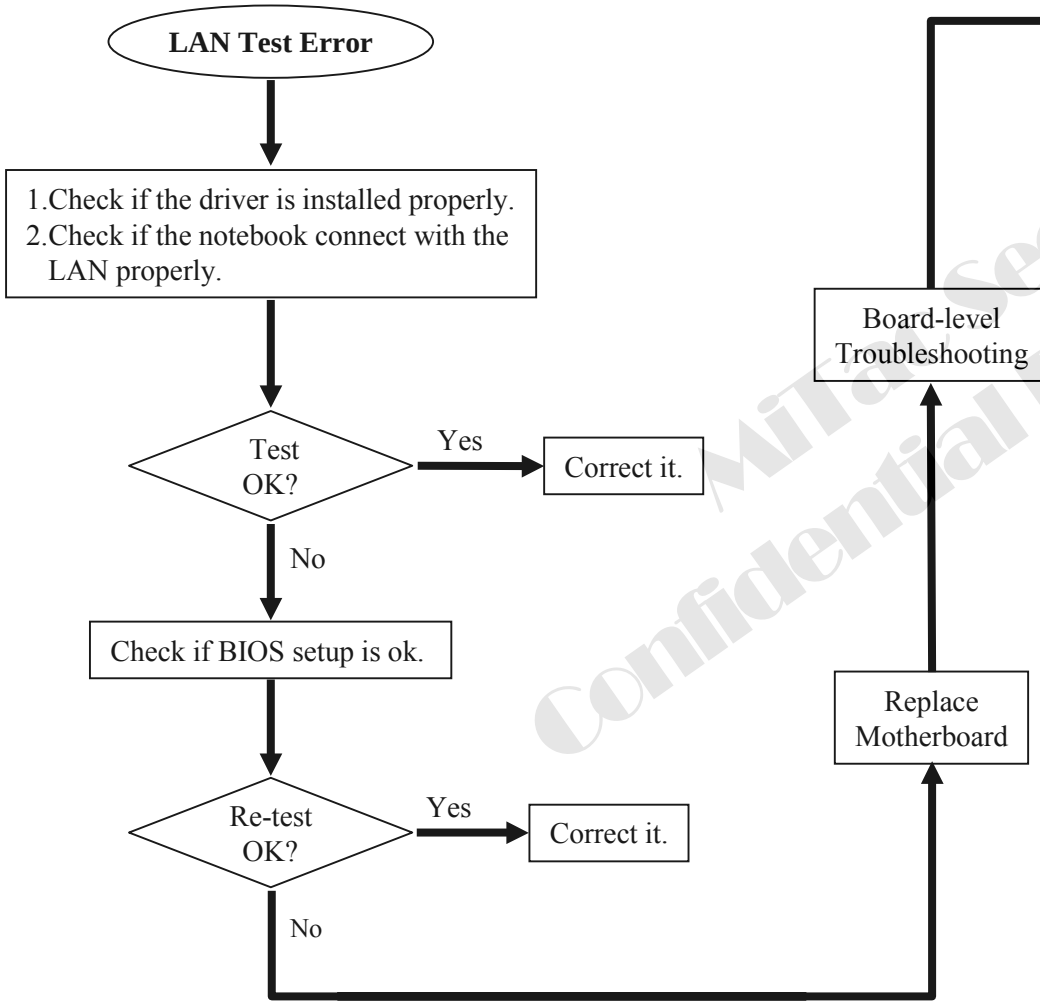
8.11 LAN Test Error

An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:	
U511	+LAN_A2.5V	PCI_GNT1#
U12	+LAN_D2.5V	PCI_PAR
U515	CARD_RI#	AD[0..31]
U509	PCICLK_LAN	CBE#[0..3]
J511	PCIRST#	RXIN+
X504	IN_PIRQE#	RXIN-
L534	PCI_REQ1	TXD+
L536	PCI_FRAME#	TXD-
Q520	PCI_DEVSEL#	EECS
Q519	PCI_TRDY#	EESK
L531	PCI_IRDY#	EEDI
L533	PCI_PME#	EEDO
L535	PCI_STOP#	
R645		
JS3		

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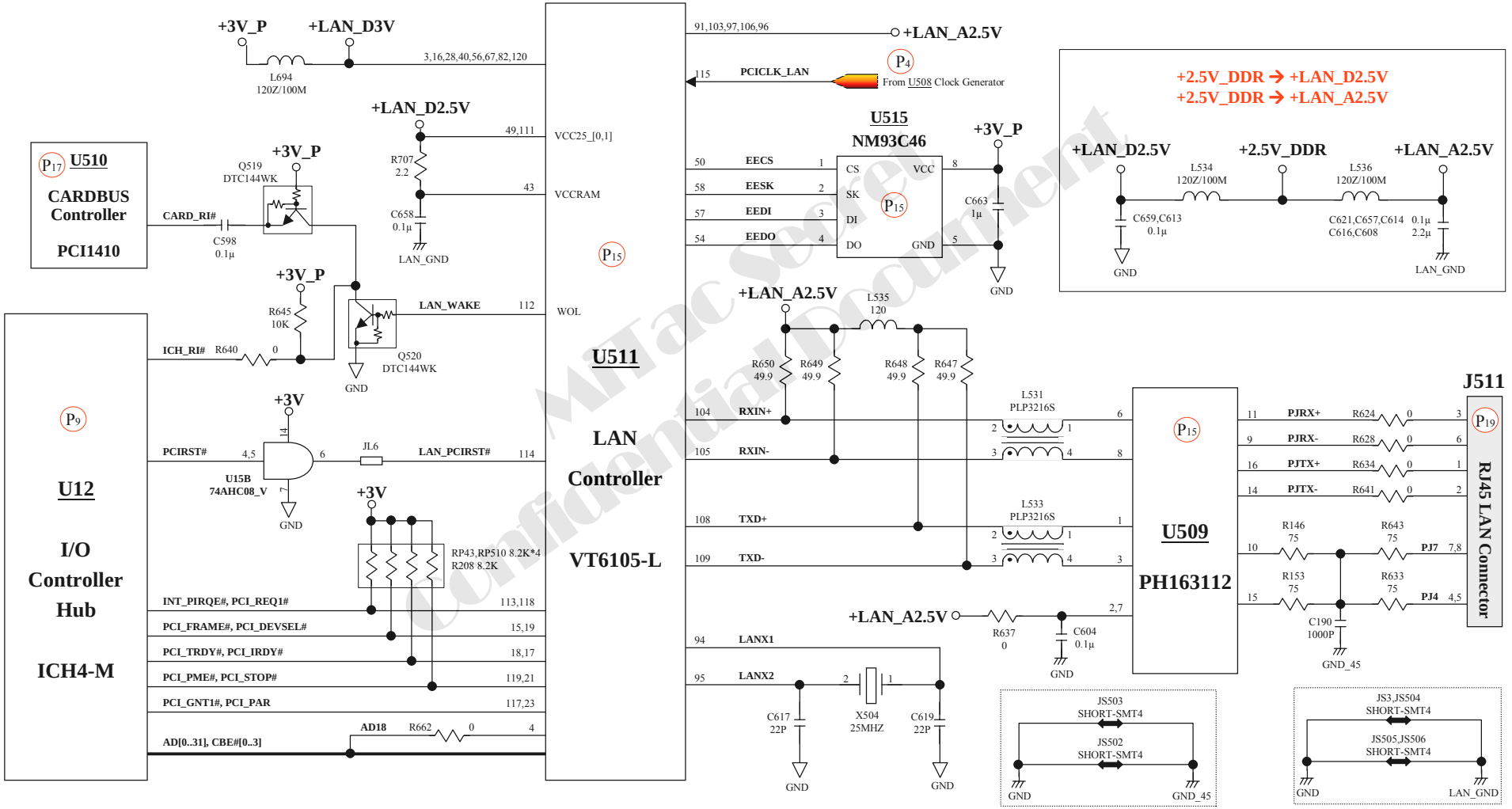
8.11 LAN Test Error

An error occurs when a LAN device is installed.



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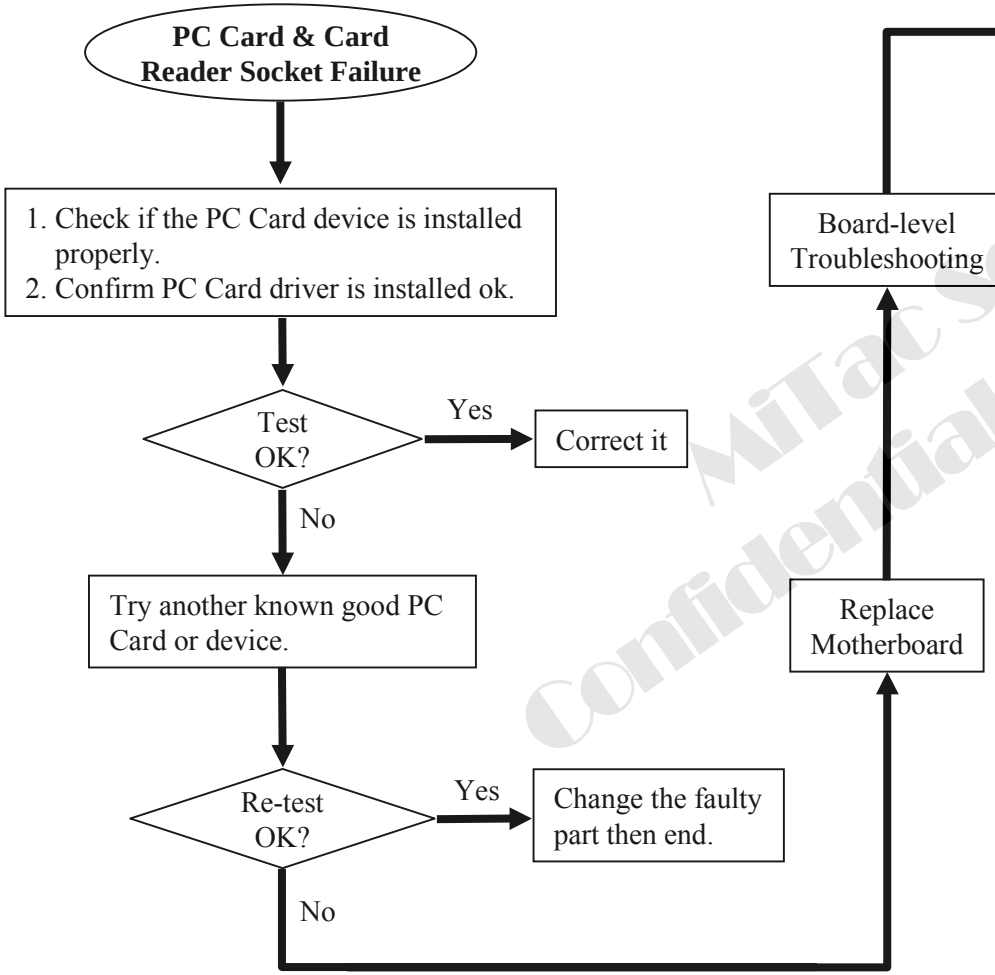
8.12 PC Card Socket Failure

An error occurs when a PC card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U12
U510
J6
U513
R819
R816
RP41
U15

Signals

PCICLK_CARD
PCIRST#
INT_PIRQB#
PCI_REQ0#
PCI_SERR#
PCI_PERR#
PCI_DEVSEL#
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCLKRUN#
PCI_PME#
PCI_GNT0#
PIC_PAR
SERIRQ
SUSB#
AD[0..31]
CC/BE#[0..3]
VCC5_EN#
VCC3_EN#
VPPD0
VPPD1

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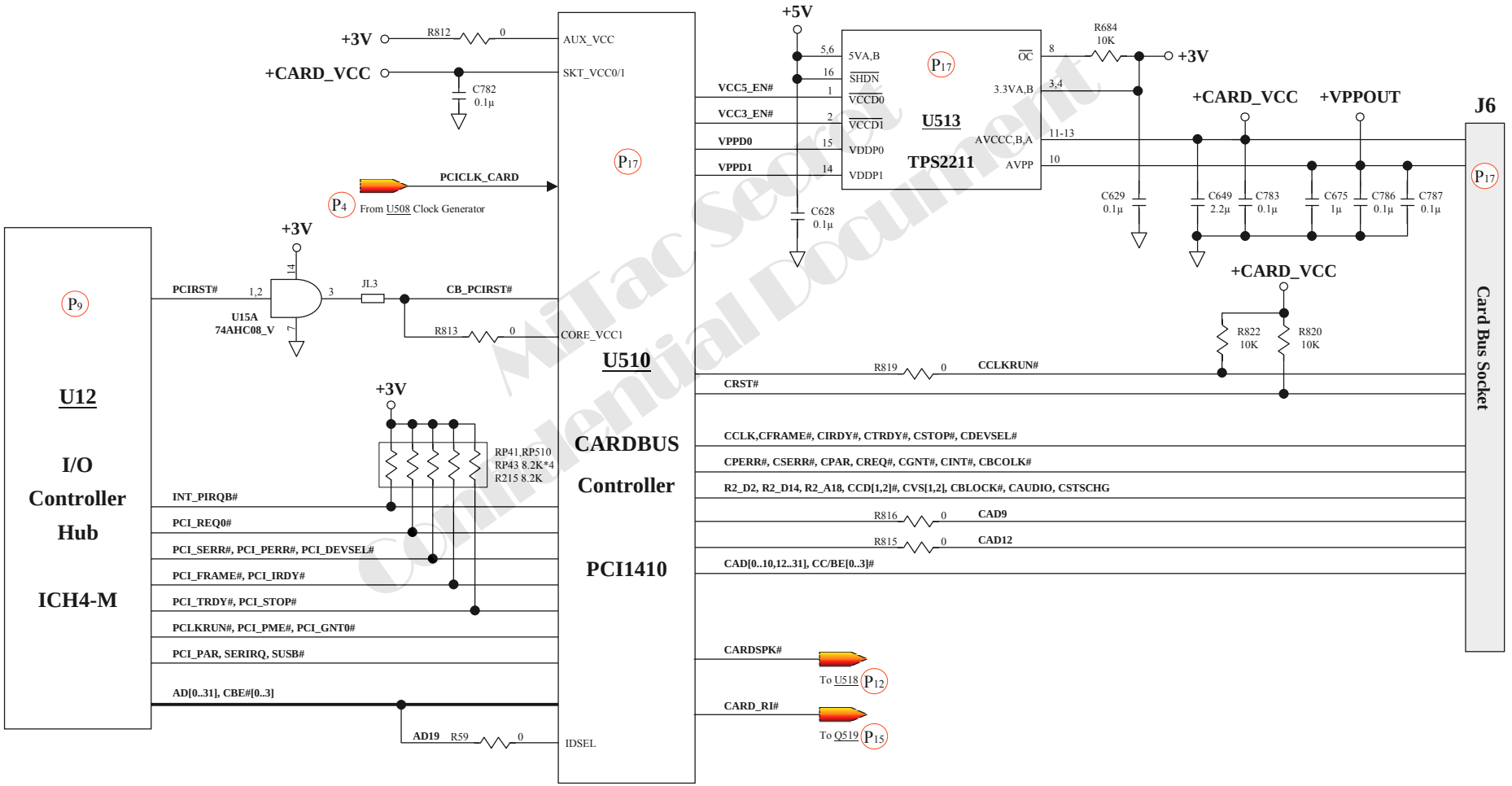
8.12 PC Card Socket Failure

An error occurs when a PC card device is installed.



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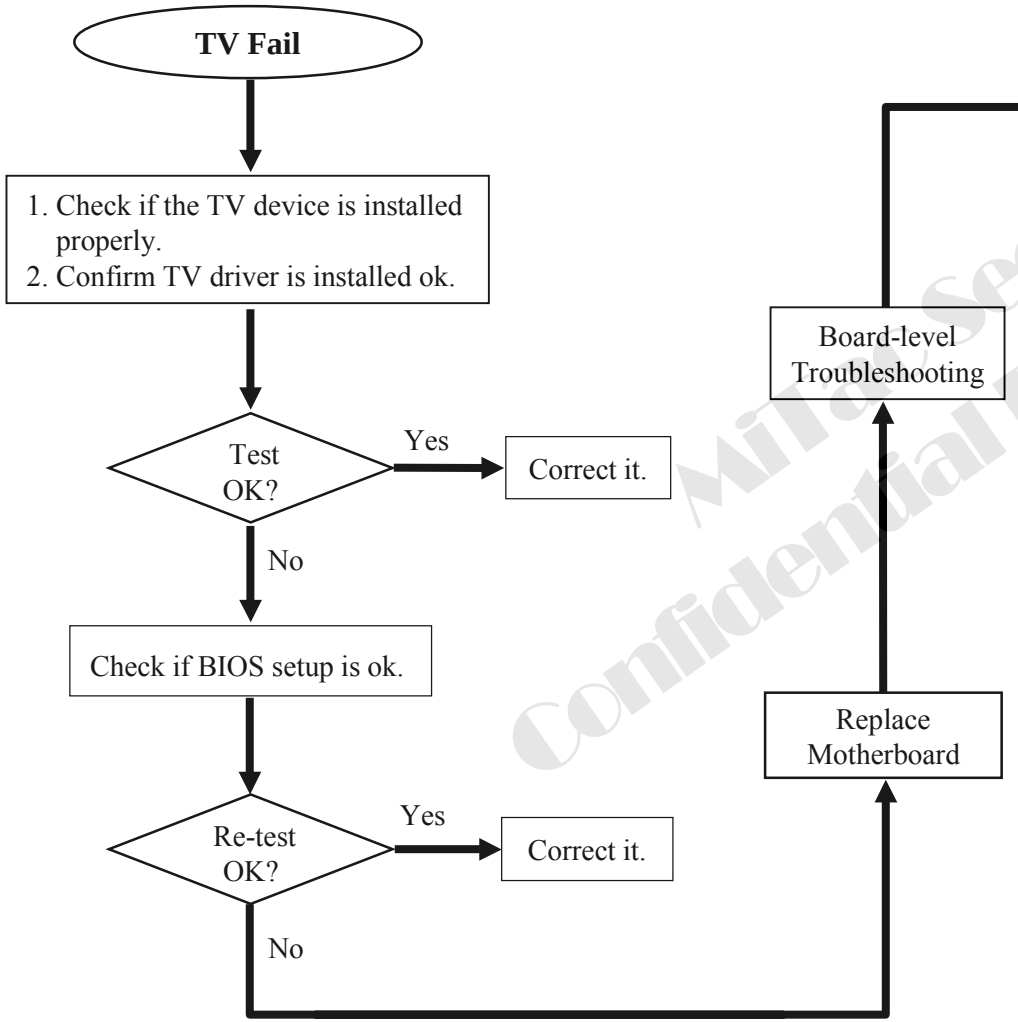
8.13 TV Test Error

An error occurs when a TV device is Connected.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U504	DVOCD[0:11]	+1.5VS
U5	DVOCHSYNC	+3VS
R29	DVOCVSYNC	
Q7	DVOCCLK	
Q8	DVOCCLK#	
R33	POUT/DET#	
R16	DVOCFLDSTL	
L501	TV_DDCK	
L502	TV_DDDA	
J501	TV_LUMA	
C502	TV_CRMA	
L509		

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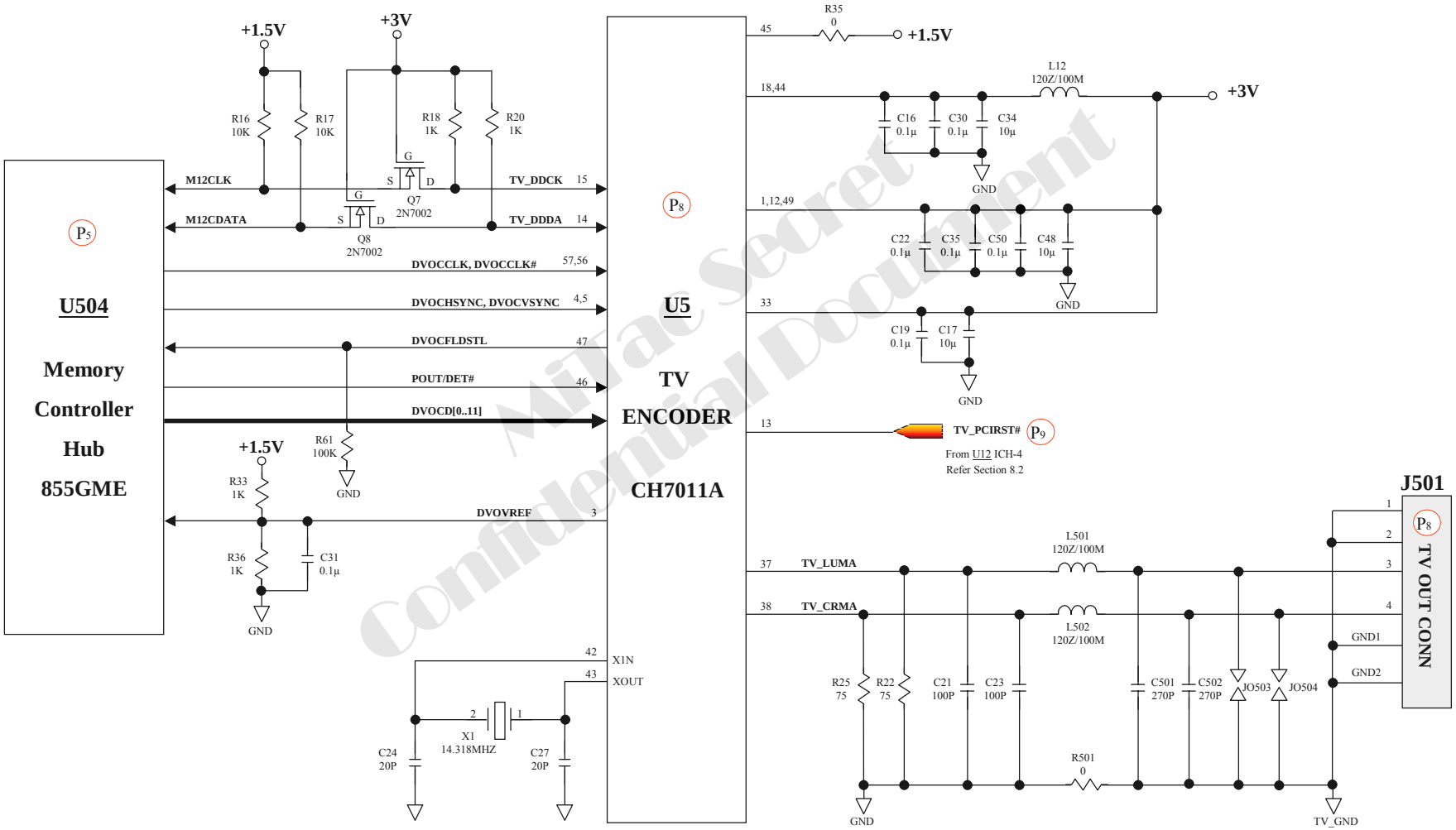
8.13 TV Test Error

An error occurs when a TV device is connected.



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9. Spare Part List

Spare Part List 1

Part Number	Description	Price(US)
221672350007	REINFORCE BRKT;50 x 50 x 830MM	
221673550007	REINFORCE BRKT;L985*50*50*T5	
221674550004	REINFORCE BRKT;L800*50*50*T5	
221677040001	BOX,AK,LYNX	
221677050003	CARD BOARD;TOP/BTM,PALLET,LYNX	
221677750002	PARTITION;MANUAL,GHARIAL-N	
221682820001	CARTON;N-B,8089	
221682850002	CARD BOARD;FRAME,PALLET,8089P	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
222670820003	PE BAG;L560*W345,7521N	
222672730001	PE BUBBLE BAG;200*240mm,AMM-9019	
224672330001	PALLET;1200x1050x135MM,MANGUSTA	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	
226600030332	SPONGE;320*290*10,CAIMAN,PWR	
227677000001	END CAP;L/R,LYNX	
227677000002	PAD;LCD/KB,LYNX	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242600000385	LABEL;27*10,LAN ID BAR CODE	

Part Number	Description	Price(US)
242600000433	LABEL;BLANK,11*5MM,COMMON	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242669600005	LABEL;LOT NUMBER,RACE	
242670800113	BFM-WORLD MARK;WINXP,7521N	
242677000027	LABEL,AK BOX,LYNX	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8	
242682800001	LABEL;AGENCY-GLOBAL,ID2,8089P	
242682800015	LABEL;BATT,11.1V/4.0AH,LI,PANASO	
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-0	S1
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L18,R236,R35,R501,R574,R585,R
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR505,PR506
271013478301	RES;4.7 ,1/4W,5% ,1206,SMT	R800
271045057101	RES;.005 ,1W,1% ,2512,SMT	PR522
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR508,PR81
271046017301	RES;.001,2W,5%,2512,CYNTEC,SMT	PR520
271046087301	RES;.008 ,2W,5% ,2512,SMT	PR509
271046407101	RES;.040 ,2W ,1% ,2512,SMT,PRC	R18A,R18B,R18C
271061000002	RES;0 ,1/16W,0402,SMT	R391,R392,R393,R394,R395,R396
271061103501	RES;10K ,1/16W,5% ,0402,SMT	R684,R818,R820,R822
271061104501	RES;100K ,1/16W,5% ,0402,SMT	R54

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9. Spare Part List

Spare Part List 2

Part Number	Description	Price(US)
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L28,L29,L30,L31,PR1,PR24,PR25
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR13,PR501,R130,R188,R78
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R52,R578,R581,R586,R67,R88
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R37
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR50,PR52,R116,R126,R520,R569
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R111,R18,R20,R33,R36,R514,R54
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R35,R39,R43
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR33,PR74
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR20,PR21,PR88,PR95,R107,R11
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R3,R4
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR2,PR34,PR40,PR80
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R7
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR17,PR18,PR38,PR42,PR504,PR
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R11,R15,R2,R38,R44,R48
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR39,PR5,PR507,PR525,PR64,PR
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R40
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R206,R718
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR15
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR73
271071127011	RES;127 ,1/16W,1% ,0603,SMT	R44
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R163
271071134701	RES;130K ,1/16W,0.1% ,0603,SMT	PR56
271071137011	RES;137 ,1/16W,1% ,0603,SMT	R14A

Part Number	Description	Price(US)
271071137271	RES;13.7K,1/16W,.1%,0603,SMT	PR10,PR62
271071141102	RES;140 ,1/16W,1% ,0603,SMT	R19
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R103,R105,R125,R158,R167,R525
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R523
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R17
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R19
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR48,PR533,PR58
271071184301	RES;180K ,1/16W,5% ,0603,SMT	R14,R765
271071196111	RES;1.96K,1/16W,1% ,0603,SMT	PR16
271071201101	RES;200 ,1/16W,1% ,0603,SMT	R234
271071201301	RES;200 ,1/16W,5% ,0603,SMT	PR57,PR61,R656
271071201301	RES;200 ,1/16W,5% ,0603,SMT	R14,R17
271071202102	RES;2K ,1/16W,1% ,0603,SMT	PR89,PR90,R566
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R12
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR29,PR30,PR4,PR529,PR531,PR
271071220101	RES;22 ,1/16W,1% ,0603,SMT	R170
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R183,R187,R221,R243,R244,R7,R
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R511,R515,R559,R560,R743,R748
271071225301	RES;2.2M,1/16W,5% ,0603,SMT	R34,R36
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR55
271071228301	RES;2.2 ,1/16W,5% ,0603,SMT	R707
271071244301	RES;240K ,1/16W,5% ,0603,SMT	R41
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR75
271071274111	RES;2.74K,1/16W,1% ,0603,SMT	PR45
271071274301	RES;270K ,1/16W,5% ,0603,SMT	R42

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9. Spare Part List

Spare Part List 3

Part Number	Description	Price(US)
271071274811	RES;27.4 ,1/16W,1% ,0603,SMT	R100,R527,R553,R595,R87
271071274911	RES;27.4 ,1/16W,1% ,0603,SMT	R616,R619,R623,R626
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R526,R563
271071301301	RES;300 ,1/16W,5% ,0603,SMT	R110,R875
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR22
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R13,R3
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R510,R572,R583,R604,R609,R611
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R145,R255,R256,R257,R258,R259
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R16,R20,R22
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R18,R21,R23
271071332302	RES;3.3K ,1/16W,5% ,0603,SMT	PR76
271071332311	RES;332K ,1/16W,1% ,0603,SMT	PR35,PR532
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR47,PR513
271071343101	RES;34K ,1/16W,1% ,0603,SMT	PR92
271071374812	RES;37.4 ,1/16W,1% ,0603,SMT	R576
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R123,R512,R513
271071391302	RES;390 ,1/16W,5% ,0603,SMT	R567,R805
271071402811	RES;40.2 ,1/16W,1% ,0603,SMT	R235,R50
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R10
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	PR526
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R1
271071471302	RES;470 ,1/16W,5% ,0603,SMT	PR14,R1,R196,R874
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R1
271071472101	RES;4.7K ,1/16W,1% ,0603,SMT	R799
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR51,PR53,R140,R148,R155,R220

Part Number	Description	Price(US)
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR63,R211,R227,R762,R91
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR503,R10,R193,R573
271071475011	RES;475 ,1/16W,1% ,0603,SMT	R142
271071487011	RES;487 ,1/16W,1% ,0603,SMT,MUS	R168
271071487311	RES;487K ,1/16W,1% ,0603,SMT	PR9
271071487811	RES;48.7 ,1/16W,1% ,0603,SMT	R177
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR37,PR7
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	PR11
271071499311	RES;499K ,1/16W,1% ,0603,SMT	PR19
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R147,R152,R580,R647,R648,R649
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R112,R122,R596,R597,R598,R601
271071511101	RES;510 ,1/16W,1% ,0603,SMT	PR54
271071549811	RES;54.9 ,1/16W,1% ,0603,SMT	R101,R79,R80,R89
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R127,R129,R169,R176,R182,R657
271071561101	RES;560 ,1/16W,1% ,0603,SMT	R570,R804
271071562201	RES;56.2K,1/16W,1% ,0603,SMT	PR31
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R45
271071563101	RES;56K ,1/16W,1% ,0603,SMT	R6
271071604111	RES;6.04K,1/16W,1% ,0603,SMT	R651
271071604112	RES;604,1/16W,1% ,0603,SMT	R104,R106
271071604811	RES;60.4 ,1/16W,1% ,0603,SMT	R615,R618,R622,R625,R96,R98
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR518
271071634111	RES;6.34K,1/16W,1% ,0603,SMT	PR530
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR12
271071681111	RES;6.81K,1/16W,1% ,0603,SMT	R21

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9. Spare Part List

Spare Part List 4

Part Number	Description	Price(US)
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R594
271071681813	RES;68.1,1/16W,1%,0603,SMT	R577
271071698311	RES;698K ,1/16W,1% ,0603,SMT	R5
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R134,R135,R146,R153,R22,R25,R
271071750311	RES;750K,1/16W,1% ,0603,SMT	PR77
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R8
271071822102	RES;8.2K ,1/16W,1% ,0603,SMT	R14B
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R138,R143,R149,R166,R173,R192
271071909101	RES;9.09K,1/16W,1% ,0603,SMT	R24
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR8
271072287011	RES;287 ,1/10W,1% ,0603,SMT	R584
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R4
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R5
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP1,RP10,RP11,RP12,RP13,RP2,1
271571560302	RP;56*8 ,16P,1/16W,5% ,1606,SMT	RP16,RP17,RP18,RP19,RP20,RP2
271586026101	RES;.02 ,2W,1%,2512,SMT	PR502,PR512
271611560301	RP;56*4 ,8P ,1/16W,5% ,0612,SMT	RP14,RP15
271611822301	RP;8.2K*4,8P ,1/16W,5% ,0612,SMT	RP38,RP41,RP43,RP510
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP512
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC17,PC501,PC62
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C14,C266,C582
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C170,C185,C191,C20,C260,C267,(
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,S	C13,C14
272002475702	CAP;4.7U ,CR,16V ,+80-20%,Y5V,08	C2
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC505

Part Number	Description	Price(US)
272005104402	CAP;.1U ,50V,+/-10%,0805,X7R,SMT	C8,PC42,PC43,PC7,PC8,PC86,PC
272005104502	CAP;.1U ,CR,50V,20%,0805,Z5U,SM	PC24,PC35,PC40
272010680301	CAP;68P,2KV,5%,1206,NPO,SMT,only	C18
272010680401	CAP;68P ,CR,2KV,10%,1206,NPO,SM	
272011106409	CAP;10U,10V,+-10%,1203,X5R,SMT,T	PC34,PC511,PC541,PC74
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C11,C111,C112,C113,C114,C115,(
272011226701	CAP;22U ,CR,10V,1206,Y5V,+80~20%	C28,C32,C40,C556,C565,C759,C8
272012105401	CAP;1U ,CR,16V ,10%,1206,X7R,S	C14A,C14B
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C539,C58,C608,C616,C649
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C802,C96
272021226701	CAP;22U ,10V,+80-20%,1210,Y5V,S	PC89,PC90
272023106002	CAP;10U,25V,M,1210,T2.8MM,X5R,SM	PC507,PC508,PC519,PC520,PC52
272023475401	CAP;4.7U ,25V ,10%,1210,X5R,SMT	C1
272030050302	CAP;5P,3KV,5%,1808,NPO,SMT,only	C19
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C157,C158,C190
272071105403	CAP;1U ,10V ,10%,0603,X5R,SMT	C10,C4
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C10,C163,C173,C175,C238,C239,(
272071332401	CAP;.33U ,10V ,10%,0603,X7R,SMT	C2
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	PC533
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C17,C6
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C12
272072104702	CAP;.1U ,16V,+80-20%,0603,Y5V,S	C139,C142,C159,C160,C161,C162
272072224402	CAP;.22U ,16V ,10%,0603,X7R,SMT	PC21
272072334701	CAP;.33U ,CR,16V ,+80-20%,0603,Y	C743,C744,C745
272072473401	CAP;.047U,16V ,10%,0603,X7R,SMT	C697

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9. Spare Part List

Spare Part List 5

Part Number	Description	Price(US)
272072474701	CAP;.47U ,16V,+80-20%,0603,Y5V,S	C1,C23,C28
272072683404	CAP;.068U ,16V ,10%,0603,X7R,SMT	C16
272073104401	CAP;.1U ,CR,25V,10%,0603,X7R,PR	C22,C7
272073104501	CAP;.1U ,25V,+80-20%,0603,Y5V,S	PC52
272073151301	CAP;150P ,CR,25V,5% ,0603,NPO,SM	PC54
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C255,C256
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C9
272073472301	CAP;4700P,CR,50V ,5% ,0603,X7R,S	C5
272075100302	CAP;10P ,CR,50V ,5%,0603,NPO,SM	C600,C603
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SM	C606
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C21,C23,C265,C504,C723,C735,P
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C20,C21
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	C2,C4,C711,C719,C763,C765,PC1
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC22,PC527,PC531,PC535
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	C11
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	C13,C3,C8
272075103403	CAP;.01U ,50V,10%,0603,X7R,SMT	C20,C21,C22
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	C182,C193,C194,C195,C196,C197
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C1,C100,C101,C102,C103,C105,C
272075104703	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C24,C26,C3,C4,C5,C6
272075200302	CAP;20P ,CR,50V ,5% ,0603,NPO,S	C24,C27
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C617,C619,C808,C809,C810
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,S	C46,C49
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	C535,PC101,PC102,PC26,PC37

Part Number	Description	Price(US)
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C15A
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C501,C502
272075339901	CAP;3.3P ,CR,50V ,+-.25PF,0603,N	C776,C777,C778,C779,C780,C781
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	C755,PC39
272075472701	CAP;4700P,50V ,+ -20%,0603,X7R,S	PC48,PC95
272101474702	CAP; .47U ,CR,10V,+80-20% ,0402,	C246,C59,C86,C89
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y	C44
272105222501	CAP;2200P,50V ,+/-20%,0402,X7R,S	C807
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C528,C766,PC517,PC518
272431157512	CAP;150U,6.3V,+/-20%,H2.8,PT ,NCC	
272431227402	CAP;220U,2V,-35/+10%,H1.9,S,SP-C	PC536,PC537,PC68,PC71,PC73,P
272431227510	CAP;220U ,TPC,4V,20%,H1.9,7343,S	PC514,PC53,PC542,PC543,PC58
272601107506	EC;100U ,6.3V,M,9.3*3.6,-55~105'	C714,C715
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C269
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP503
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CP504
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L531,L533
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L3,L33,L34,L35,L4,L546
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L10,L11,L12,L13,L14,L16,L19,L2
273000150001	FERRITE CHIP;220OHM/100MHZ,2012,	L1
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	L21,L23,L24,L25,L26,L27,L525,L
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L38,L41,L44,L47
273000150332	FERRIET CHIP;120OHM/100MHZ,2012,	L2,L37,L49,L50,L510,L541,L6,PI
273000500084	CHOKE COIL;400UH(REF),D.2*1,10.5	L529

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Part Number	Description	Price(US)
273000610019	FERRITE ARRAY;130OHM/100MHZ,3216	FA1
273000990018	INDUCTOR;10uH,CDRH125,SUMIDA,SMT	PL503,PL504
273000990024	INDUCTOR;47uH,CDRH127,SUMIDA,SMT	PL506
273000990127	INDUCTOR;IHLP5050CE-01-0.68uH,VI	PL509
273000990129	INDUCTOR;4.7UH,20%,D124C,H4.5,TO	PL510,PL511
273001050028	XSFORMER;10/100 BASE,LF-H41S,SMT	U509
273001050126	XFMR;CI8.5,25T/2150T,292mH,Varni	T1
274010800405	XTAL;8Mhz,30PPM,16PF,8*4.5,2P,SM	X2
274011431409	XTAL;14.318MHZ,16PF,50PPM,8*4.5,	X1
274011431414	XTAL;14.318MHZ,32PF,50PPM,8*4.5,	X501
274012500415	XTAL;25MHZ,20PF,30PPM,8.0*4.5,SM	X504
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X3
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,	U1
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,	U15
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U2
282574108002	IC;74AHC1G08,SINGLE AND GATE,SOT	U524,U525
282574132001	IC;74AHCT1G32,SINGLE OR GAT,SOT2	U518
283467490001	IC;FLASH,512K*8,FWH,SST49LF004A,	
283467490002	IC;FLASH,512K*8,FWH,W39V040FAP,P	
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	U2
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BIT	U515
284500101006	IC;ALC101,AC97 CODEC,LQFP,48P,SM	U519
284500522001	IC;855GME GMCH,NORTH BRIDGE,BGA,	U504
284501410007	IC;PCI1410A,PCI/CARDBUS,PQFP,144	U510
284502996001	IC;LP2996,DDR,NS,PSOP8,SMT	

Part Number	Description	Price(US)
284506105001	IC;VT6105LOM, PCI LAN CONTROLLER	U511
284507011001	IC;CH7011A,TV ENCODER,LQFP,64P	U5
284507460002	IC;ADT7460,TEMPERATURE MTR,QSOP,	U523
284508807001	IC;AME8807AEHA,600mA,CMOS LDO,AM	PU3
284520715001	IC;PLL207-151,CLOCK GEN,TSSOP,56	U508
284582801044	IC;FW82801DBM,ICH4-M,BGA,421P	U12
284583950002	IC;W83L950D-Ver.C,LPC_KBC,LQFP,8	
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	U3
286100212001	IC;TPA0212,AMPLIFIER,TSSOP,24P,S	U18
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU8
286104073001	IC;MAX4073F,I-SENSE AMP,SOT23,6P	PU501
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	
286300317010	IC;AMS3107C, VOLTAGE REGULATOR,	U10
286300338001	IC;SC338,FET CTRL,SC,MSOP-10	PU14
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ14
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU5
286300690001	IC;GMT690B,RESET CIRCUIT,2.93V,S	U503
286300809009	IC;MAX809STR,RESET CIRCUIT,2.93V	
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	U1
286301117021	IC;AMS1117,VOL REGULATOR,1A,SOT-	U16,U4
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	U5
286301907001	IC;MAX1907A,PWM CONTROLLER,40-QF	PU4
286302211004	IC;TPS2211A,POWER INTERFACE SW,S	U513
286302996001	IC;G2996,DDR,GMT,SOP8FD,SMT	PU10
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	PU13,PU2

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Part Number	Description	Price(US)
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U521,U522
288100014007	DIODE;SS14,40V,1A,SMA	
288100018003	DIODE;UDZS18B,ZENER,18V,SOD-323,	ZD3,ZD4
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D2
288100034004	DIODE;SSA34,40V,3A,SMA	PD508,PD509,PD510,PD511
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D509,D510,D8
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D3,D507
288100056003	DIODE;BAW56,70V,215mA,SOT-23	
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD1,ZD2,ZD5
288100056017	DIODE;BAW56LT1,70V,215MA,SOT-23,	D1,D4,D5,D6,PD1,PD5
288100070006	DIODE;BAV70LT1,70V,225MW,SOT-23,	D506,D511,PD501,PD503
288100099001	DIODE;BAV99,70V,450MA,SOT-23	
288100099012	DIODE;BAV99LT1,70V,450MA,SOT-23,	D611,D612,D613,PD506,PD507
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	D503,PD4,PD512
288101040006	DIODE;SBM1040,10A,SCHOTTKY,POWER	PD504
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D7,PD3
288105520001	DIODE;BZV55-C20,ZENER,5%,SOD-80,	PD2
288105524003	DIODE;BZV55-C24,ZENER,5%,SOD-80,	PD502
288114148004	DIODE;1N4148WS,75V,200mW,SOD-323	D1
288200112002	TRANS;BSH112,N CHANNEL FET,ESD	
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	
288200144002	TRANS;DTA144WK,PNP,SMT	
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	

Part Number	Description	Price(US)
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ9
288202237002	TRANS;MUN2237T1,NPN,SOT-23,SMT,O	PQ11,Q12,Q510,Q519,Q520
288202240001	TRANS;MUN2240T1,NPN,SOT-23,ON	Q1,Q15,Q18,Q19,Q2,Q20,Q5,Q52
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q11,Q13,Q14,Q16,Q512,Q524
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	
288203904022	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q518
288204406001	TRANS;AO4406,N-MOS,.0165OHM,SO8	PU506,PU507
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SM	PQ4,PQ5,PQ501,PQ6
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,	Q2A,Q3C
288204788001	TRANS;SI4788CY,P-MOS,5A1.8~5.5V,	U1,U501
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU1,PU11,PU503,PU6,PU7
288204800004	TRANS;SI4800,7A,30V,33mOHM,SO8	
288204807001	TRANS;AO4807,DUAL PMOS,5A,SO8	PU505
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU12,PU504
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	U3
288204900001	TRANS;AO4900,DUAL N-MOSFET WITH	PU502,PU9
288207788001	TRANS;FDS7788,18A,30V,5mOHM,SO8	PU509,PU510
288208107001	TRANS;TPC8107,13A/30V,P-MOSFET,S	
288221371002	TRANS;MUN2137T1,PNP,SMT,ON	PQ13
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	Q527,Q528
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ES	PQ1,PQ10,PQ12,PQ15,PQ16,PQ2
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000001206	CON;MINI PCI SOCKET,P124,QTC,C10	J504
291000011101	CON;HDR,MA,11P*1,1.25,ST,SMT	J3
291000012022	CON;HDR,MA,10P*2,1MM,H4.25,ST,SM	J1

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Part Number	Description	Price(US)
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	
291000020206	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A	J2,J503,J508,J516
291000020221	CON;HDR,MA,11P*1,1.25MM,R/A,ACES	
291000021104	CON;HDR,MA,11P*1,1.25,R/A,3811Y-	CN1
291000023008	CON;HDR,FM,15P*2,0.8MM.H5,R/A,SM	J515
291000024421	CON;HDR,MA,22P*2,R/A,SUYIN,20038	J514
291000025028	CON;HDR,FM,25P*2,R/A,SUYIN,80094	J510
291000141204	CON;FPC/FFC,12P,0.5MM,H=2,ACES,S	J5
291000152603	CON;FPC/FFC,26P,1MM,R/A,KBD,SMT	J4
291000256827	CON;IC CARD,68P,0.635MM,62596-00	J6
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J505
291000616803	IC SOCKET;BANIAS m-FCBGA478P, MO	U506
291000622007	CON;DIMM,R/A,200P,.6,H9.2,REVERS	J509
291000810607	CON;PHONE JACK,6P,SG-2SJ-S820	J8,J9
291000811008	CON;PHONE JACK,2 IN 1,7.0MM,ALLT	J511
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D15,D16,D17,D18,D19
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	LED1
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	LED2
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	LED3,LED5
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	LED4,LED6
295000010014	FUSE;1.1A/6V,POLY SWITCH,PTC,SMD	F1,F501
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1
295000010020	FUSE;NORMAL,7A/24VDC,1206,SMT	PF501
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,S	F503
295000010048	FUSE;0.5A/15V,POLY SWITCH,SMD	F502

Part Number	Description	Price(US)
295000010105	FUSE;1A,NORMAL,1206,SMT	F2,PF2
295000010110	FUSE;NORMAL,2.5A/63VDC,3216,SMT	F3
295000010120	FUSE;FAST,1.5A,63V,1206,SMT,PRC	F1
295000010149	FUSE;FAST,1.5A,63VDC,1206,SMT,04	
297004010001	SW;PUSH BUTTOM,5P,SPST,12VDC,50m	SW2,SW6,SW7
297140200002	SW;COVER SWITCH,SPST,.1A,30V,4P,	SW1
310111103011	THERMISTOR;10K,1%,RA,DISK,103AT-	T1
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC504,PC525,PC528
316677000002	PCB;PWA-LYNX/BATTERY BD,PWR	
316682200001	PCB;PWA-INVERTER BD (DA-1A08-B);	R0C
316682800001	PCB;PWA-8089P/MOTHER BD	R01
322677000003	CABLE;FFC,T/P,LYNX	
323767720004	DDR SODIMM MODULE;256MB,77.10634	
324180786386	IC,CPU,BANIAS,1.3GHZ,MICRO-FCPGA	
331000007005	CON;BATTERY,7P,2.5MM,H9,R/A,DIP,	PJ502
331000007019	CON;BATTERY,7P,2.5MM,25032A-07GI	
331000008068	CON;USB,FM,4P*2,R/A,MOLEX,67298-	J506,J507
331660020005	DIMM SOCKET;DDR SODIMM 200P, CA0	J512
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J502
331870004021	CON;MINI DIN,4P,R/A,SUYIN,35144A	J501
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	PJ501
332110020042	WIRE;#20,UL1007,70MM,RED,PRC	
332110020067	WIRE;#20,UL1007,40MM,BLACK,PRC	
332110020089	WIRE;#20,UL1007,L105mm,RED,PRC	
332110020096	WIRE;#20,UL1007,40MM,BLACK,YIYI;	

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Part Number	Description	Price(US)
332110020104	WIRE;#20,UL1007,105MM,RED,YIYI;P	
332110020108	WIRE;#20,UL1007,70MM,RED,YIYI;PW	
332110026007	WIRE;#26,UL1007,80MM,YELLOW	
332110026124	WIRE;#26,UL1007,80MM,YELLOW,YIYI	
332110026134	WIRE;#26,UL1007,135MM,BLACK,PRC,	
332110026135	WIRE;#26,UL1007,40MM,ORANGE,PRC,	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
333050000107	SHRINK TUBE;UL,600V,105'C,ID2.5*	
333050000120	SHRINK TUBE;600V,105'C,D0.8*9MM,	
335152000044	CFM-BAT;FUSE THERMAL 98'C	
335152000062	FUSE;LR4-730,POLY SWITCH,PRC	
335612000004	THERMAL CUTOFFS;378,8A/50VDC,139	
338536010006	BATTERY;LI,3.6V/2.0AH,18650,PANA	
339115000046	MICROPHONE;-60dB+-2dB,D6.0*H2.7,	MIC1
340677000001	SPEAKER ASSY;L,LYNX	
340677000008	COVER ASSY;CPU,LYNX	
340677000009	SHIELDING ASSY;HDD,LYNX	
340677000011	COVER ASSY;HDD,LYNX	
340677000013	SPEAKER ASSY;R,LYNX	
340677000037	HOLDER;PCMCIA FCI-62599,BLACK,LY	J6
340677000040	HEATSINK ASSY;BANIAS,LYNX	
340677000044	HEATSINK ASSY;BANIAS,MPT,LYNX	
340677000081	BEZEL ASSY;COMBO,LITEON,LSC-2408	
340682600010	HOUSING;ASSY,8689	
340682800001	SHIELDING ASSY;COVER,8089P	

Part Number	Description	Price(US)
340682810001	COVER ASSY;8089P	
340682810004	COVER ASSY;KB,8089P	
340682810005	COVER ASSY;LCD,14",8089P	
340682810007	HOUSING ASSY;LCD,14",8089P	
341677000002	SPRING;SCREW,HEATSINK,LYNX	
342503200003	CONTACT PLATE;W4L18T0.15,7521/GR	
342503400004	CONTACT PLATE;W5L45T0.13,7170LI,	
342503400006	CONTACT PLATE;W5L45T0.13,7170LI,	
342503400007	CONTACT PLATE;W5L45T0.13 ,1/3T,7	
342665500010	CFM-SUYIN,S-STANDOFF,#4-40H4.8,N	
342672200010	BRACKET;CD-ROM,8500	
342673100025	CONTACT PLATE;W5L46T0.13 ,2T,806	
342677000005	BRACKET;LCD 14"QDI,L,LYNX	
342677000006	BRACKET;LCD 14"QDI,R,LYNX	
342677000014	SMT NUT;A40M20-50,EMI STOP,LYNX	MTG501,MTG502
342677000016	HINGE;LCD14 L,LYNX	
342677000017	HINGE;LCD14 R,LYNX	
342677000019	CONTACT PLATE;W5L76T0.13 ,1/3T,L	
342677000022	HINGE;LCD14L,LYNX,(SZS CHINA)	
342677000023	HINGE;LCD14R,LYNX,(SZS CHINA)	
342677000026	HINGE;LCD14 L,LYNX-AMD(BANIAS),1	
342677000027	HINGE;LCD14 R,LYNX-AMD(BANIAS),1	
343677100001	HEATSINK;NORTHBRIDGE,BANIAS,LYNX	
344503100304	DUMMY;D18L65,BATT ASSY,7521C	
344677000006	COVER;DDR,LYNX	

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Part Number	Description	Price(US)
344677000007	COVER;MINIPCI,LYNX	
344677000012	COVER;HINGE,LYNX	
344677000022	COVER;BATTERY,LYNX	
344677000023	HOUSING;BATTERY,LYNX	
344682810004	BUTTON;T/P,8089P	
345677000006	GASKET;AUDIO,LYNX	
345677000007	GASKET;DC_JACK,LYNX	
345677000008	GASKET;TV_OUT,LYNX	
345677000009	GASKET;USB,LYNX	
345677000010	GASKET;RJ_COMBO,LYNX	
345677000024	CONDUCTIVE TAPE;INSULATOR MB,LYN	
345677000029	SPONGE;HEATSINK NB,BANIAS,LYNX	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BL	
346503400503	INSULATOR;BATT ASSY,W7L13,8175	
346669900004	INSULATOR;INVERTER,7170	
346670500014	INSULATOR;MDC,TETRA	
346677000009	INSULATOR;FOR 3CELL DOUBLE-FA,LY	
346677000010	INSULATOR;W8L45, DOUBLE-FA,LYNX,	
346677000012	MYLAR;COVER,LCD,LYNX	
346677000016	SPONGE;RTC,LYNX	
346677000020	THERMAL PAD;DDR,LYNX	
346677000026	INSULATOR;DDR,LYNX	
346677000027	INSULATOR;PCMCIA,LYNX	
346677000028	INSULATOR;SINGLE-FA,FOR PCB-A,LY	

Part Number	Description	Price(US)
346677000029	INSULATOR;SINGLE-FA,FOR PCB-B,LY	
346677000030	INSULATOR;BATT ASSY,POLY,W30L64,	
346677000031	INSULATOR;FOR 3 CELLS,SINGLE-FA,	
346677000032	INSULATOR;BATT ASSY,THERMAL FUSE	
346677000033	INSULATOR;M/B,HEATSINK,BAINAS,LY	
346677000034	INSULATOR;M/B,BAINAS,LYNX	
346677000037	INSULATOR;SPEAKER,LYNX	
346677000042	AL FOIL;LCD,BANIAS,LYNX	
346677000043	SHIELDING;NB,BANIAS,LYNX	
346677000044	INSULATOR;W8L45T0.8, DOUBLE-FA,L	
346682600005	INSULATOR;T/P-BUTTON,8689	
346867700001	FILM;PROTECT FOR APOLLON BATTERY	
347105045025	GASKET;1,05,045,025	
347108020015	GASKET;1,08,020,015	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000	
361400003003	JET-MELT ADHESIVES;3478-Q,5/8in*	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
365350000003	SOLDER WIRE;0.8MM,SN43/PB43/BI14	
370102010204	SPC-SCREW;M2L2,NIW/NLK,K-HD	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL	

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Part Number	Description	Price(US)
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102610303	SPC-SCREW;M2.6L3,KHD,D4.4,t0.45,	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
373101722501	T-SCREW;B,M1.7,L2.5,KHD(+),T0.5,	
411682200001	PWA;PWA-INVERTER BD,DA-1A08-B,PW	
411682200002	PWA;PWA-INVERTER BD,SMT,DA-1A08-	
411682200003	PWA;PWA-INVERTER BD,SMT TOP,DA-1	
411682200004	PWA;PWA-INVERTER BD,SMT BOT,DA-1	
411682800012	PWA;PWA-8089/BATT PANASONIC,6CEL	
411682800013	PWA;PWA-8089/BATT PANASONIC,6CEL	
411682810001	PWA;PWA-8089P,MB	
411682810002	PWA;PWA-8089P,T/U	
411682810003	PWA;PWA-8089P,MB,SMT	
412672300001	PCB ASSY;FAX MODEM 56K,MDC56S-I,	
412673400008	PCB ASSY;MINI-PCI,TYPE IIIB,INTE	
412682200001	PCB ASSY;INVERTER BD,DA-1A08-B,P	

Part Number	Description	Price(US)
413000020416	LCD;HT14X19-100,TFT,14.1",LVDS,X	
416268282001	LT PF;14",ID2,HYDIS,HT14X19-100,	
422677000005	WIRE ASSY;INVERTER,LYNX	
422677000006	WIRE ASSY;MDC.LYNX	
422677000008	WIRE ASSY;BATT TO MB,FOR LYNX,MO	
422677000011	WIRE ASSY;MDC.LYNX,KAI CHI	
422677000012	WIRE ASSY;LCD 14",HYUNDAI,LYNX	
422681400031	WIRE ASSY;ANTENNA,MPT,CALYPSO	
422681400032	WIRE ASSY;ANTENNA,HANNSTAR,CALYP	
431682820001	CASE KIT;8089P,ID2	
441682800075	BATT ASSY;8089/10.8V,4AH,PANASON	
441682820001	LCD ASSY;14",ID2,HYDIS,HT14X19-1	
442672600031	AC ADPT ASSY;19V,3.16A,DELTA,706	
442677000031	TOUCH PAD MODULE;TM41PUF1311-2	
442682800001	BATT ASSY;10.8V/4.0AH,LI,PANASON	
451677000091	HDD ME KIT;LYNX-AMD	
451682800051	LABEK KIT;ID2,N-B,8089P	
451682800071	ROM ME KIT;8089	
451682820001	LCD ME KIT;14",ID2,HYDIS,HT14X19	
451682820031	HOUSING KIT;8089P,ID2	
461682800012	PACKING KIT;8089/10.8V,4AH,PANAS	
461682810001	PACKING KIT;N-B,8089P	
481682810001	F/W ASSY;SYS/VGA BIOS,8089P	U512
481682810002	F/W ASSY;KBD CTRL,8089P	U7
523405320072	HDD DRIVE,40GB,2.5",IC25N040ATMR	

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9. Spare Part List

Spare Part List 12

Part Number	Description	Price(US)
523430061007	DVD COMBO DRIVE;24x24x8X24,LSC24	
523468280032	HDD ASSY;40G,IC25N040ATMR04-0,HG	
523468300001	DVD COMBO ASSY;24X,LITEON,LSC-24	
526268282001	LTXNX;8089P/4HAI/40M/1US0/O5D3B/	
531020237826	KBD;88,US,K011718M4,8089P	
541668281031	AK;8089P,UTILITY ONLY	
541668281033	AK;BOX,8089P,UTILITY ONLY	
565168281001	S/W;CD ROM,SYSTEM DRIVE,8089P	
600100010005	SOLDER WIRE;63/37,0.8,NA,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
622200000008	TAPE;CARTON,2.5"W,30M/RL,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
627207522141	CAP;220P ,50V ,10%,0603,X7R,SMT	C25
628820014401	TRANS;DTA144EKA,PNP,100MA,50V,SO	Q6,Q7
		P/N: 526268282001

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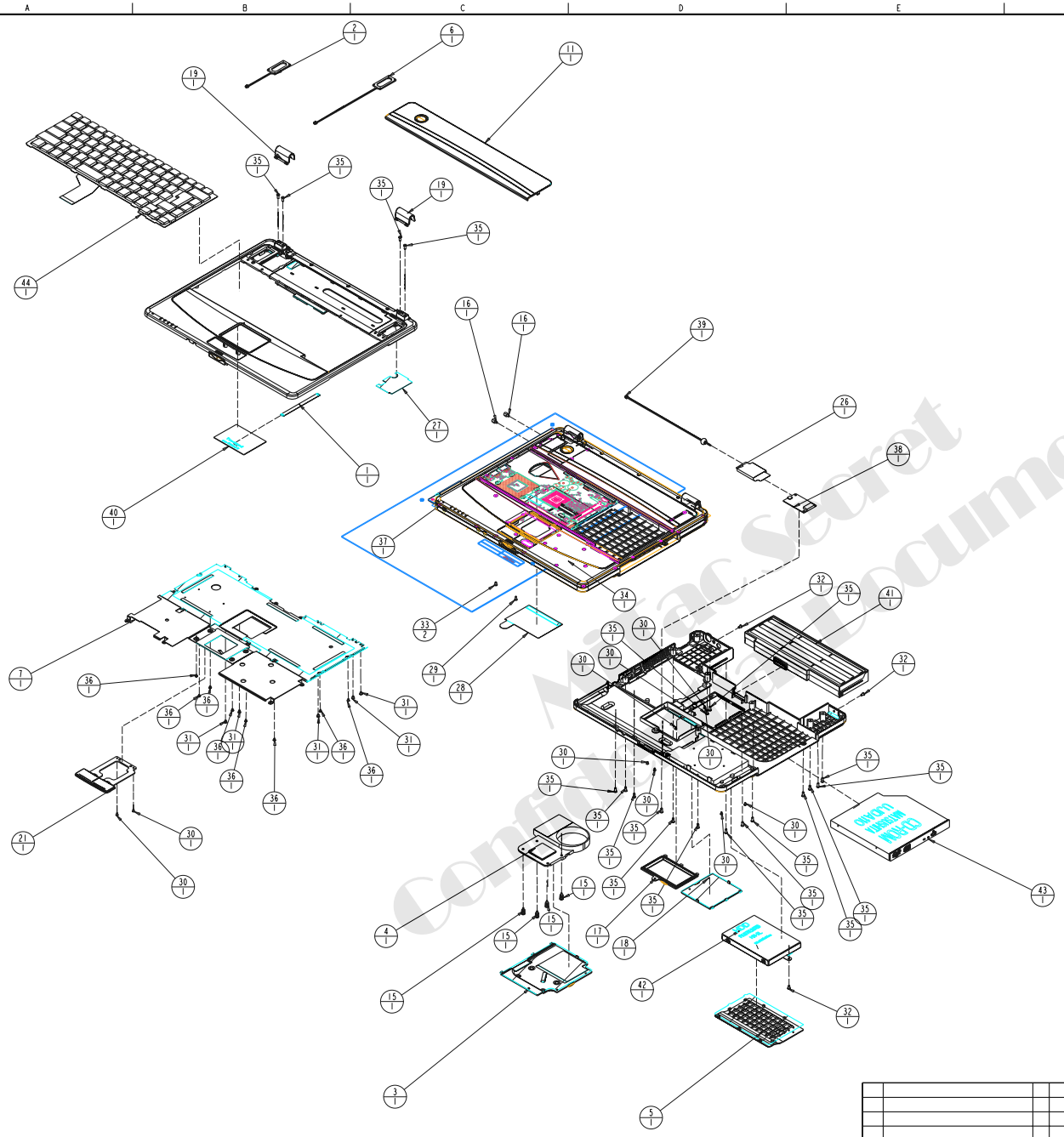

ITEM	PART NO	PART NAME	Q'TY	TYPE
1	322677000003	CABLE;FFC,T/P,LYNX	1	PART
2	340677000001	SPEAKER ASSY;L,LYNX	1	ASSEMBLY
3	340677000008	COVER ASSY;CPU,LYNX	1	ASSEMBLY
4	340677000010	HEATSINK ASSY;LYNX	1	ASSEMBLY
5	340677000011	COVER ASSY HDD,LYNX	1	ASSEMBLY
6	340677000013	SPEAKER ASSY;R,LYNX	1	ASSEMBLY
7	340677100001	SHIELDING ASSY;COVER,P4M,LYNX	1	ASSEMBLY
8	340682600010	HOUSING;ASSY,8689	2	ASSEMBLY
9	340682600018	COVER ASSY;CPU,8689	1	ASSEMBLY
10	340682810001	COVER;ASSY,8089P	2	ASSEMBLY
11	340682810004	COVER;ASSY,KB,8089P	1	ASSEMBLY
12	340682840011	COVER;ASSY,KB,ID4,8089P	1	ASSEMBLY
13	340682840013	COVER ASSY;CPU,ID4,8089P	1	ASSEMBLY
14	340682840014	COVER ASSY;HDD,ID4,8089P	1	ASSEMBLY
15	341677000002	SPRING-SCREW-HEATSINK-LYNX	4	PART
16	342665500008	CFM-SUYIN; S-STANDOFF	2	PART
17	344677000006	COVER;DDR,LYNX	1	PART
18	344677000007	COVER;MINIPCI,LYNX	1	PART
19	344677000012	COVER;HINGE,LYNX	2	PART
20	344682600005	INSULATOR;T/P,BATT,8689	1	PART
21	344682810004	BUTTON;T/P,8089P	1	PART
22	344682840017	BUTTON;T/P,ID4,8089P	1	PART
23	344682840019	COVER;DDR,ID4-8089P	1	PART
24	344682840022	COVER;MINIPCI,ID4,8089P	1	PART
25	344682840025	COVER;HINGE,ID4,8089P	2	PART
26	346670500014	INSULATOR;MDC,TETRA	1	PART
27	346677000037	INSULATOR;SPEAKER,LYNX	1	PART
28	346677000038	INSULATOR;DDR,LYNX	1	PART
29	370102010502	SPC-SCREW;M2L5,NIB,K-HD,t0.8,NLK	1	PART
30	370102030301	SPC-SCREW; M2L3,K-HEAD,1,NIB,NLK	10	PART
31	370102610303	SPC-SCREW;M2.6L3,KHD,D4.4t0.45,N	5	PART
32	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	3	PART
33	370102610405	SPC-SCREW; M2.6L4 K-HEAD,NIW	2	PART
34	370102610501	SPC-SCREW;M2.6L5,NIW,K-HD,NYLOK	1	PART
35	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	19	PART
36	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	8	PART
37	411677110001	PWA;PWA-LYNX-BANIAS,NEC-CI,MOTHE	1	ASSEMBLY
38	412672300001	PCB ASSY;FAX MODEM 56K,MDC56S-1,	1	PART
39	422677000006	WIRE ASSY;MDC,LYNX	1	ASSEMBLY
40	442164900021	TOUCH PAD MODULE;90425	1	PART
41	442677000001	BATT ASSY;11.1V/6.0AH,LI,PAN,Lyn	1	ASSEMBLY
42	451677000091	HDD ME KIT;LYNX-AMD	1	ASSEMBLY
43	451677010005	COMBO DVD ME KIT;KME,UJDA740-MT3	1	ASSEMBLY
44	531020237661	KBD;89,US,K0117I8MI,LYNX	1	PART
45			3	PART

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ITEM	CONTENTS OF CHANGE	BVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL ± RANGE	M1	M2	S1	S2	P1	P2	C	B
0-6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6-30	0.1	0.2	.15	.25	0.1	.15	1	.15
30-80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80-180	.15	0.3	.25	.45	0.4	0.8	3	.25
180-315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315-800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	11-Dec-03	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.30	DRAWING NAME	HOUSING KIT;8089P,IDI		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD 451 6828 10031 R 00A		

MiTAC Technology Corp.

model name:SYSTEM-ASSY-EXP-8089 | file name:8089P

SHEET NO. 1 of 1

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8089P_R01

Project Code : G115

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PAGE08 TV Encoder
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PAGE10 ICH4-M USB_HUB_GPIO_AC97_IDE(2)
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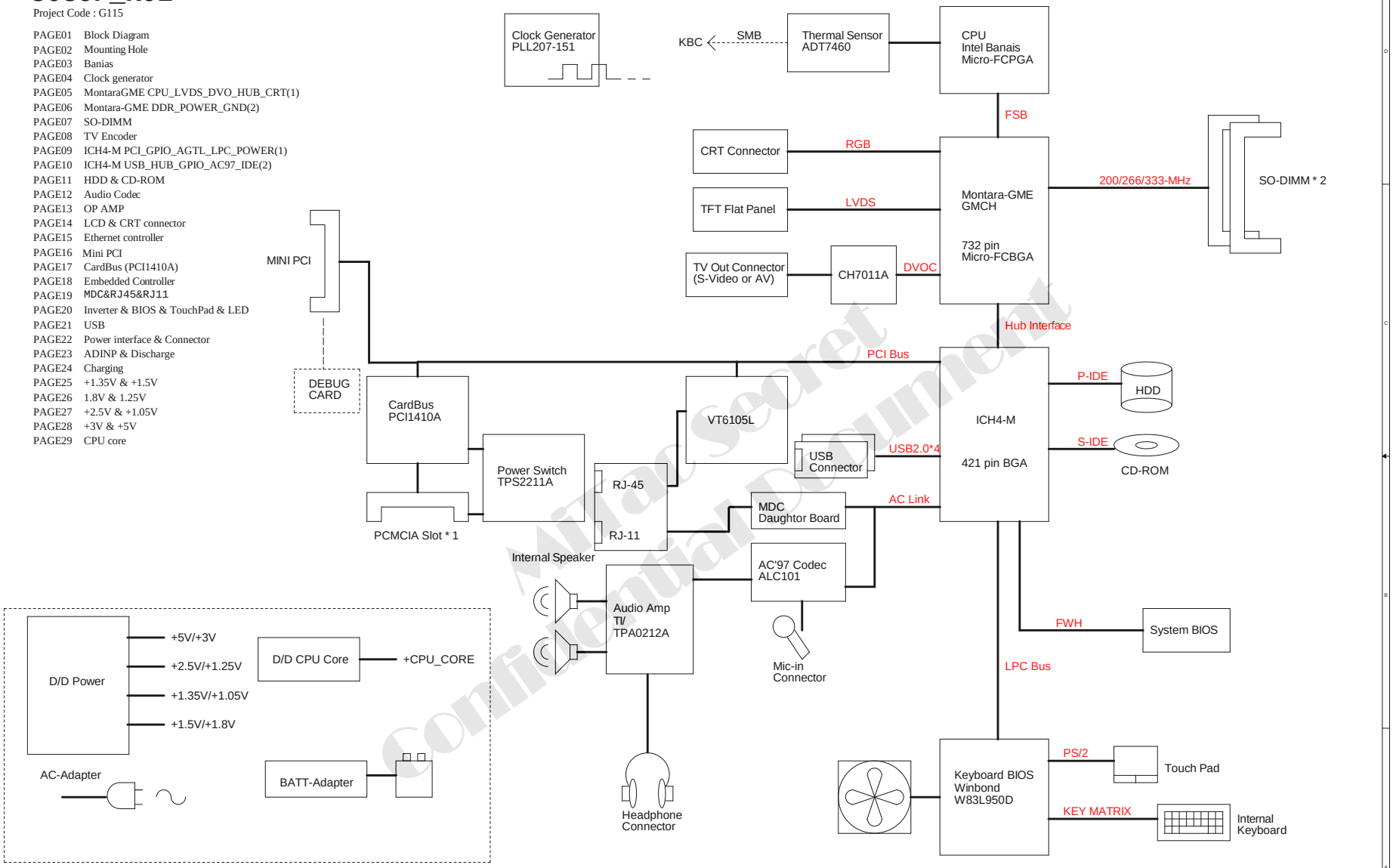
PAGE23 ADINP & Discharge
PAGE24 Charging
PAGE25 +1.35V & +1.5V
PAGE26 1.8V & 1.25V
PAGE27 +2.5V & +1.05V
PAGE28 +3V & +5V
PAGE29 CPU core



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Title: **Block Diagram**

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VT6105L
IDSEL: AD18
PCI REQ1#
PCI GNT1#
PCI INTE#

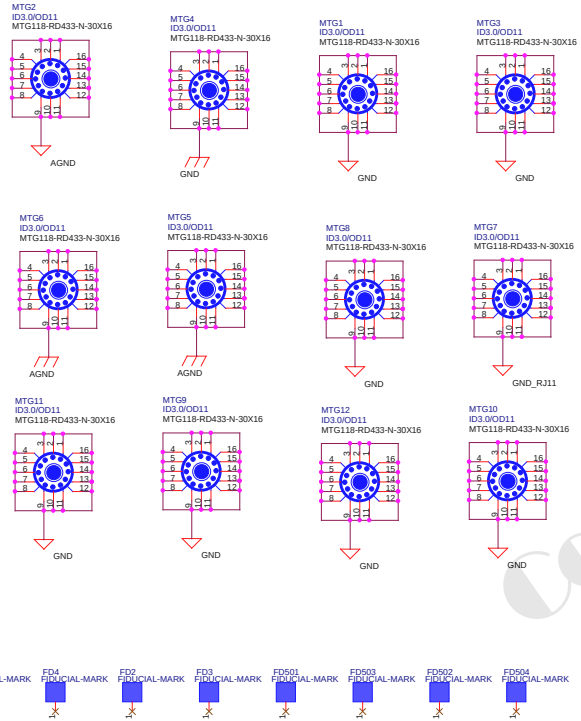
Mini PCI
IDSEL: AD17
PCI REQ2#
PCI GNT2#
PCI INTD# INTF#

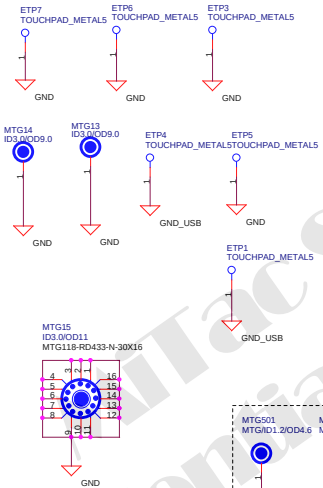
PCI1410A
IDSEL: AD19
PCI REQ0#
PCI GNT0#
PCI INTB#

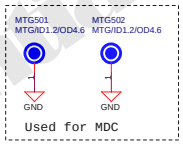
8089P Stack Up

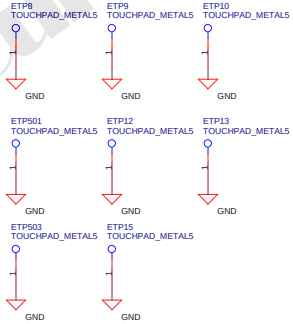
	Comp	0.5 oz	Cu
4 mil			
	GND	0.5 oz	Cu
6 mil			
	In1	0.5 oz	Cu
7 mil			
	In2	0.5 oz	Cu
6 mil			
	PWR	0.5 oz	Cu
7 mil			
	In3	0.5 oz	Cu
6 mil			
	GND	0.5 oz	Cu
4 mil			
	Solder	0.5 oz	Cu

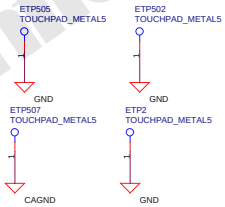
REV	Change detail	DATE	ECR No.
R00	Initail release (base on Lynx Banias)		
R0A	1. Remove power VDD5S and add SVDD3 for software standby power. 2. Fix 5 KBC signals pull hi voltage from VDD3 to SVDD3. 3. Fix signal "LPCCLK_KBC" from 48MHz to 33MHz. 4. Reserve signal "SUPERIO_48M" for software debug. 5. Fix signal "HINIT#" pull hi voltage from Vcore to +VCCP. 6. Fix Inverter LED power from VDD5S to VDD3. 7. Add Celeron_Banias CPU power saving circuit. 8. Fix Vcore circuit short issue. 9. Signal BAT_T and BAT_V pull hi voltage to SVDD3 in page 18 and page 23. 10.Inverter power add a PMOS to turn on power. 11.Signal "Wireless_LED#" control changed from KBC to BIOS. 12.+1.5V_P and +1.35_P power turn on control changed form SUSB# to PWRON_1.35V_1.5V. 13.KBC add 2 NA pins. 14.USB circuit change resistor from 33K & 47K to 390 & 560 to speedy discharge time. 15.Remove D506 to disable ENABLE_BKLT controled by LID#. 16.Remove U17 for cost down. 17.Use 24.576MHz oscillator instead of codec clock which come from clock gen. to fix audio EMI issue. 18.Use 0 ohm to instead of bead between GND & AGND in audio for EMI recommendation.		
R01	1. Change SUSB# pull hi from VDD3 to SVDD3 for support RTC wake up. 2. Correct NUM#,CAP#,SCROLL# pull hi from +5V to +3V. 3. Change R234,R235 resistance for stable VDD1.5 voltage. 4.Use internal clock from clock gen. to instead X'tal. 5.Add C507 to fix audio noise. 6. Change PC95 to let 1.05V later. 7.Add U524,U525 to improve VESA quality. 8.Change X501 to fix clock timing.	2004/2/5	G115930372

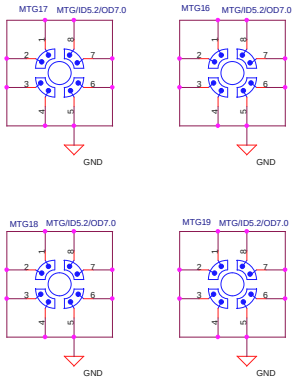












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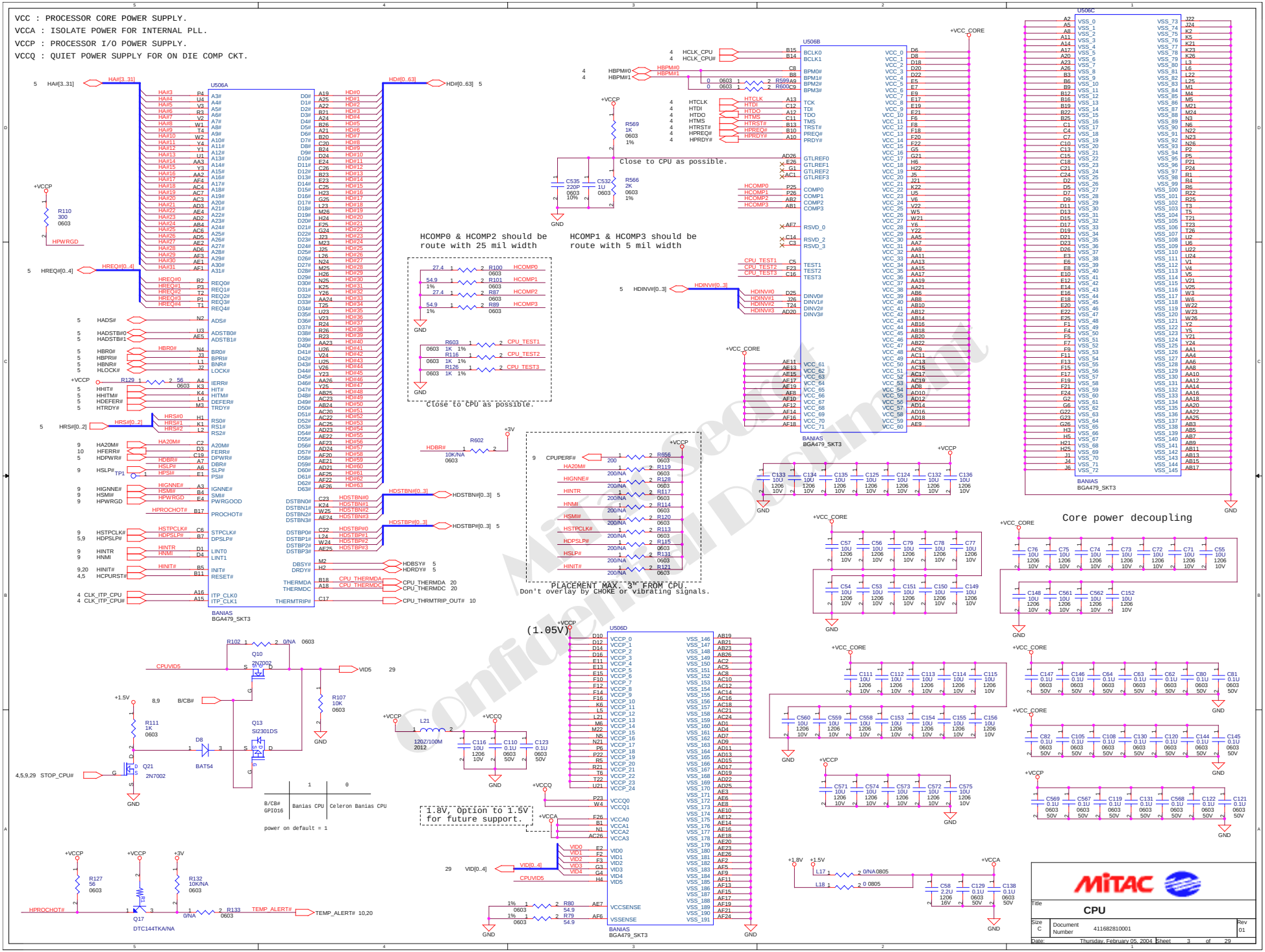
VCC : PROCESSOR CORE POWER SUPPLY.
VCCA : ISOLATE POWER FOR INTERNAL PLL.
VCCP : PROCESSOR I/O POWER SUPPLY.
VCCQ : QUIET POWER SUPPLY FOR ON DIE COMP CKT.
HCOMP0 & HCOMP2 should be route with 25 mil width
HCOMP1 & HCOMP3 should be route with 5 mil width
Close to CPU as possible.
Close to CPU as possible.
PLACEMENT MAX. 3" FROM CPU.
Don't overlay by CHOKE or vibrating signals.
Core power decoupling
1.8V, Option to 1.5V for future support.
B/CB# GPIO16
Banias CPU
Celeron Banias CPU
power on default = 1
U506A
U506B
U506C
U506D
BANIAS BGA479_SKT3
CPU
Title
Size C
Document Number 411682810001
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VID 5 4 3 2 1 0	VCC-Core
0 0 0 0 0 0	1.708
0 0 0 0 0 1	1.692
0 0 0 0 1 0	1.676
0 0 0 0 1 1	1.660
0 0 0 1 0 0	1.644
0 0 0 1 0 1	1.628
0 0 0 1 1 0	1.612
0 0 0 1 1 1	1.596
0 0 1 0 0 0	1.580
0 0 1 0 0 1	1.564
0 0 1 0 1 0	1.548
0 0 1 0 1 1	1.532
0 0 1 1 0 0	1.516
0 0 1 1 0 1	1.500
0 0 1 1 1 0	1.484
0 0 1 1 1 1	1.468
0 1 0 0 0 0	1.452
0 1 0 0 0 1	1.436
0 1 0 0 1 0	1.420
0 1 0 0 1 1	1.404
0 1 0 1 0 0	1.388
0 1 0 1 0 1	1.372
0 1 0 1 1 0	1.356
0 1 0 1 1 1	1.340
0 1 1 0 0 0	1.324
0 1 1 0 0 1	1.308
0 1 1 0 1 0	1.292
0 1 1 0 1 1	1.276
0 1 1 1 0 0	1.260
0 1 1 1 0 1	1.244
0 1 1 1 1 0	1.228
0 1 1 1 1 1	1.212

VID 5 4 3 2 1 0	VCC-Core
1 0 0 0 0 0	1.196
1 0 0 0 0 1	1.180
1 0 0 0 1 0	1.164
1 0 0 0 1 1	1.148
1 0 0 1 0 0	1.132
1 0 0 1 0 1	1.116
1 0 0 1 1 0	1.100
1 0 0 1 1 1	1.084
1 0 1 0 0 0	1.068
1 0 1 0 0 1	1.052
1 0 1 0 1 0	1.036
1 0 1 0 1 1	1.020
1 0 1 1 0 0	1.004
1 0 1 1 0 1	0.988
1 0 1 1 1 0	0.972
1 0 1 1 1 1	0.956
1 1 0 0 0 0	0.940
1 1 0 0 0 1	0.924
1 1 0 0 1 0	0.908
1 1 0 0 1 1	0.892
1 1 0 1 0 0	0.876
1 1 0 1 0 1	0.860
1 1 0 1 1 0	0.844
1 1 0 1 1 1	0.828
1 1 1 0 0 0	0.812
1 1 1 0 0 1	0.796
1 1 1 0 1 0	0.780
1 1 1 0 1 1	0.764
1 1 1 1 0 0	0.748
1 1 1 1 0 1	0.732
1 1 1 1 1 0	0.716
1 1 1 1 1 1	0.700

Place close to CPU socket within 2".

001 →

FS2	FS1	FS0	CPU	3V66[5:0]	PCI*
X	0	0	166.66	66.66	33.33
X	0	1	100.00	66.66	33.33
X	1	0	200.00	66.66	33.33
X	1	1	133.33	66.66	33.33
Mid	0	0	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/2	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved

0:0V
1:3.3V
UNIT: MHz

Layout note: Place crystal within 500 mils of CLK Gen.

U508 PLL207-151 TSSOP56

U507 ICS91718/NA SO8

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Title: Clock generator
Size: C
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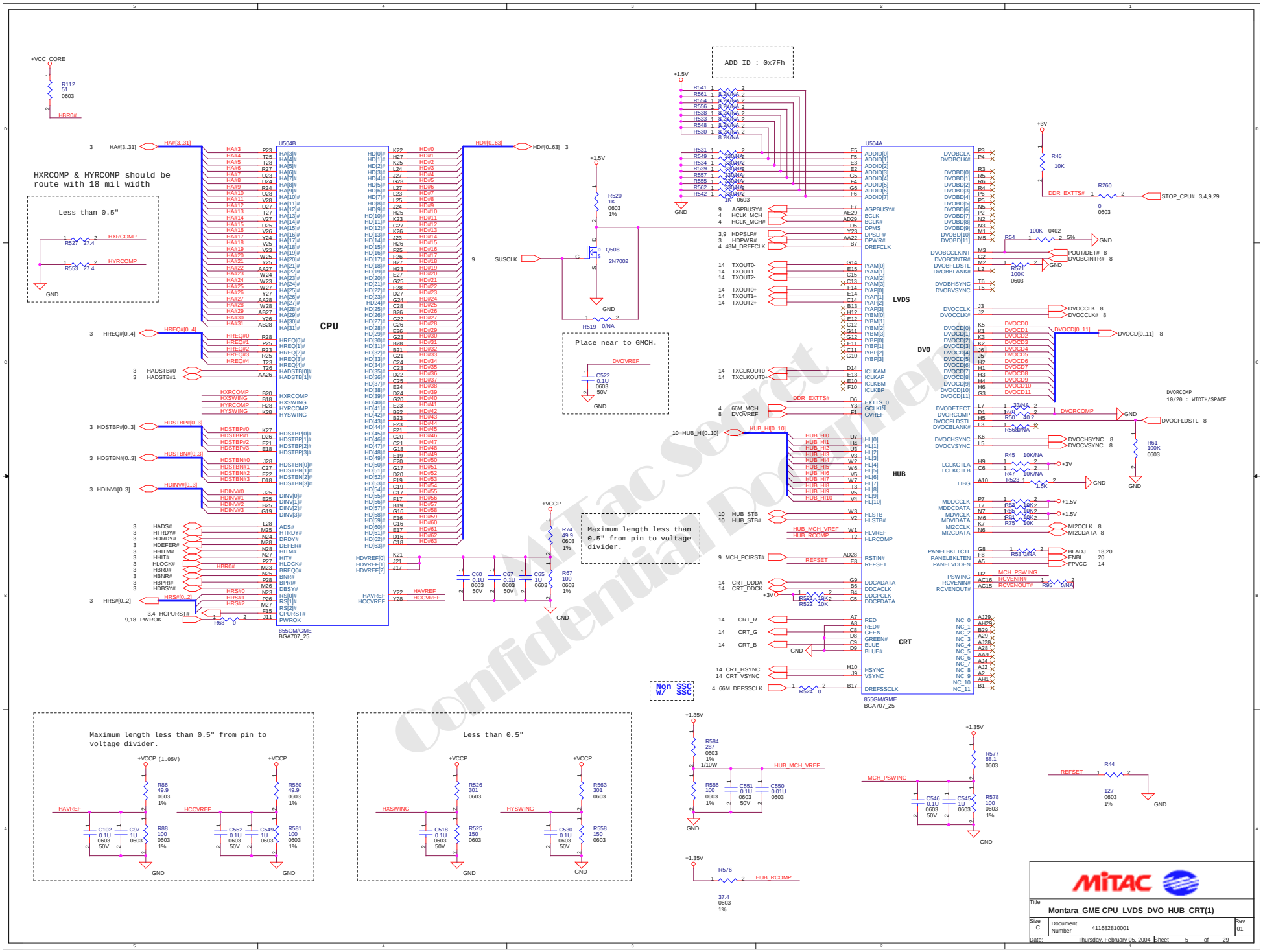

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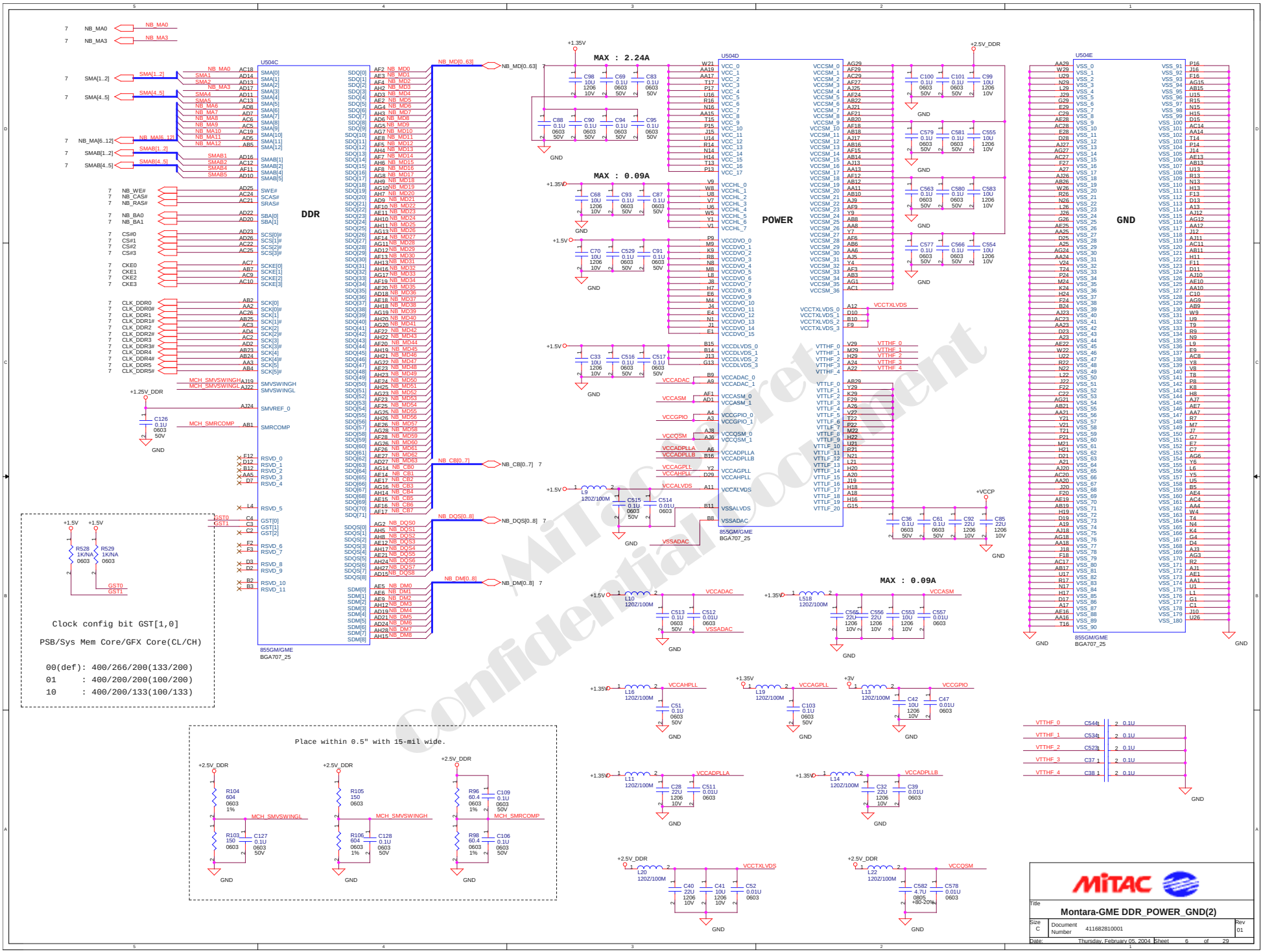

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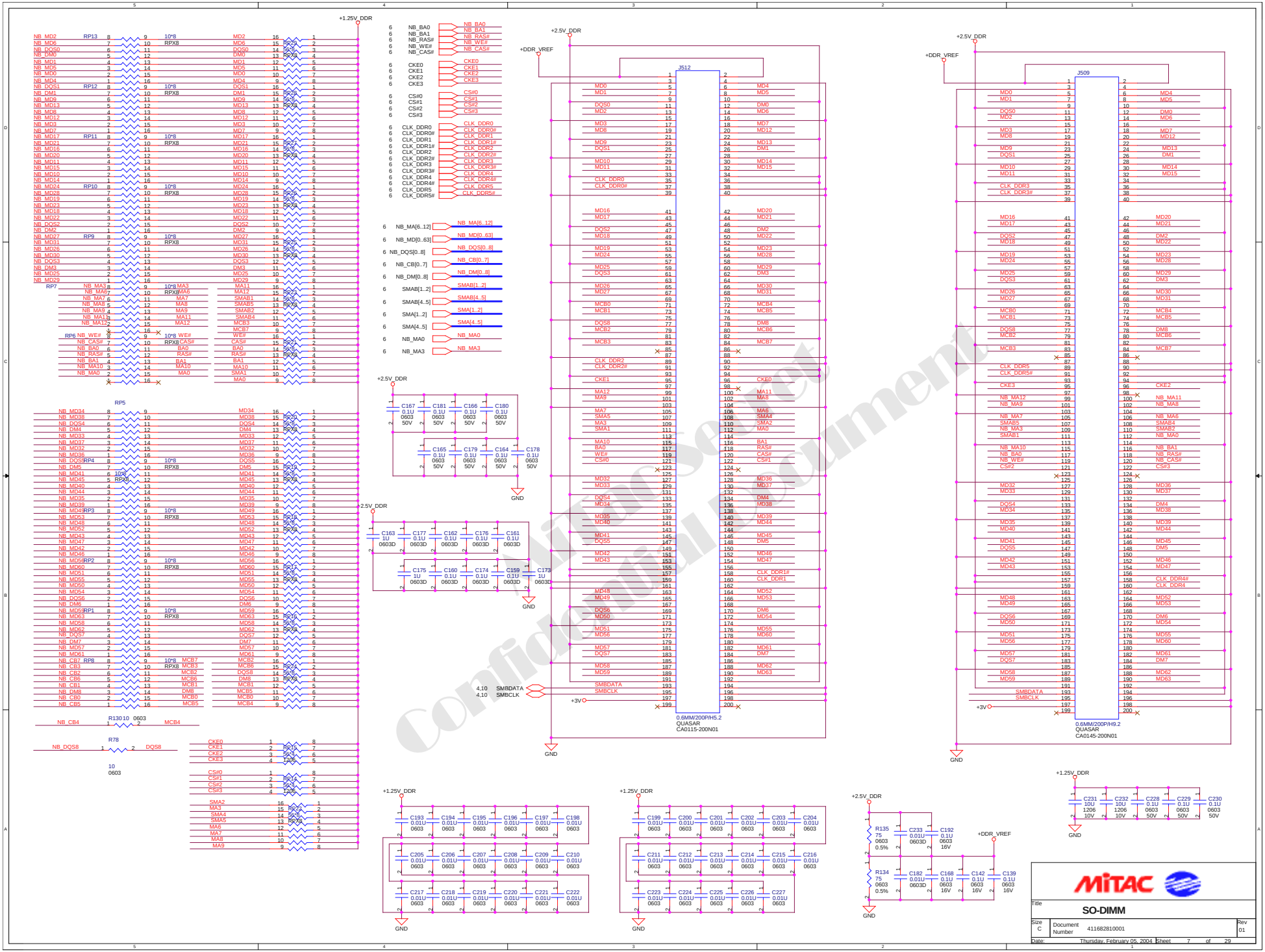

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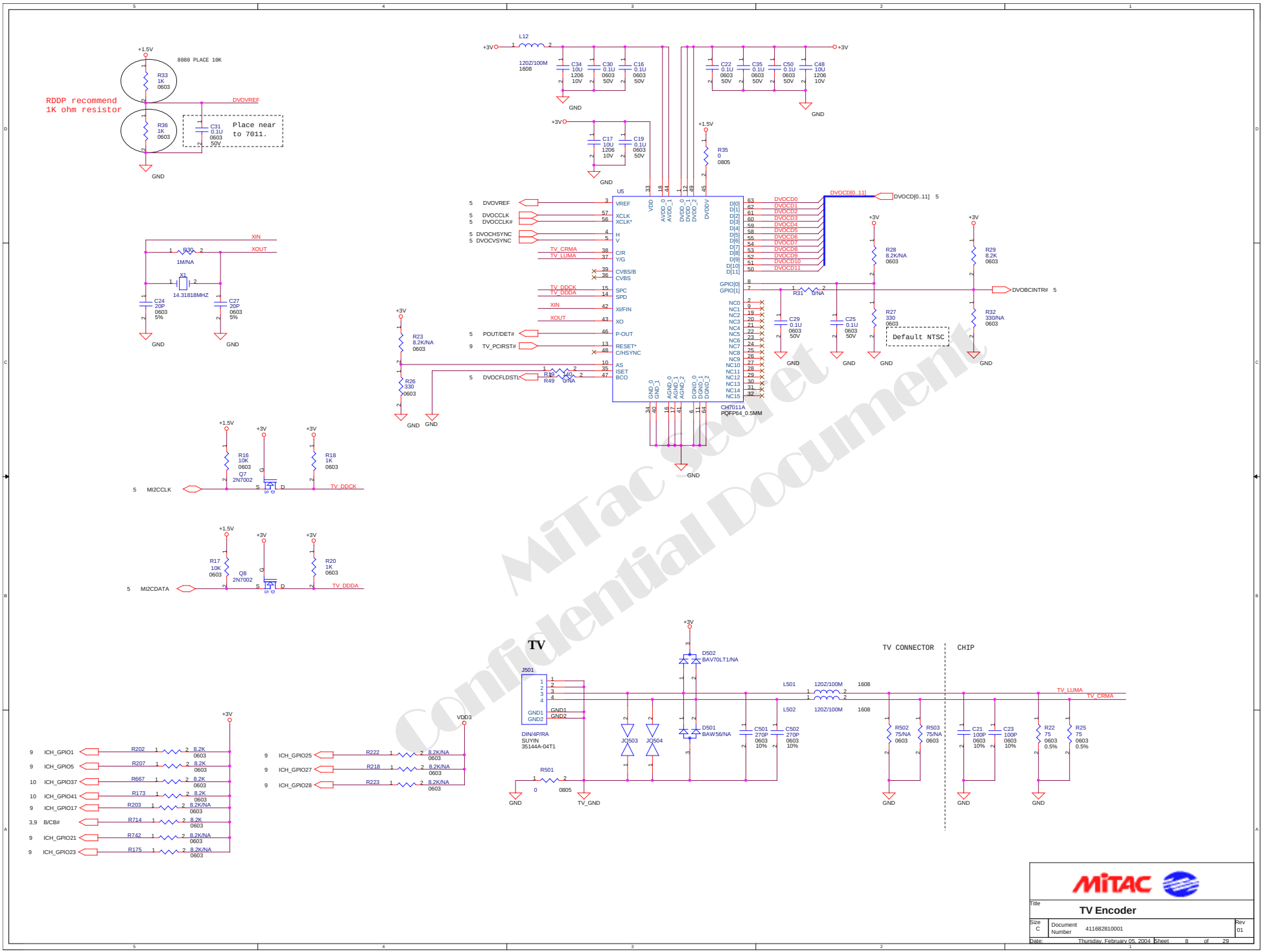

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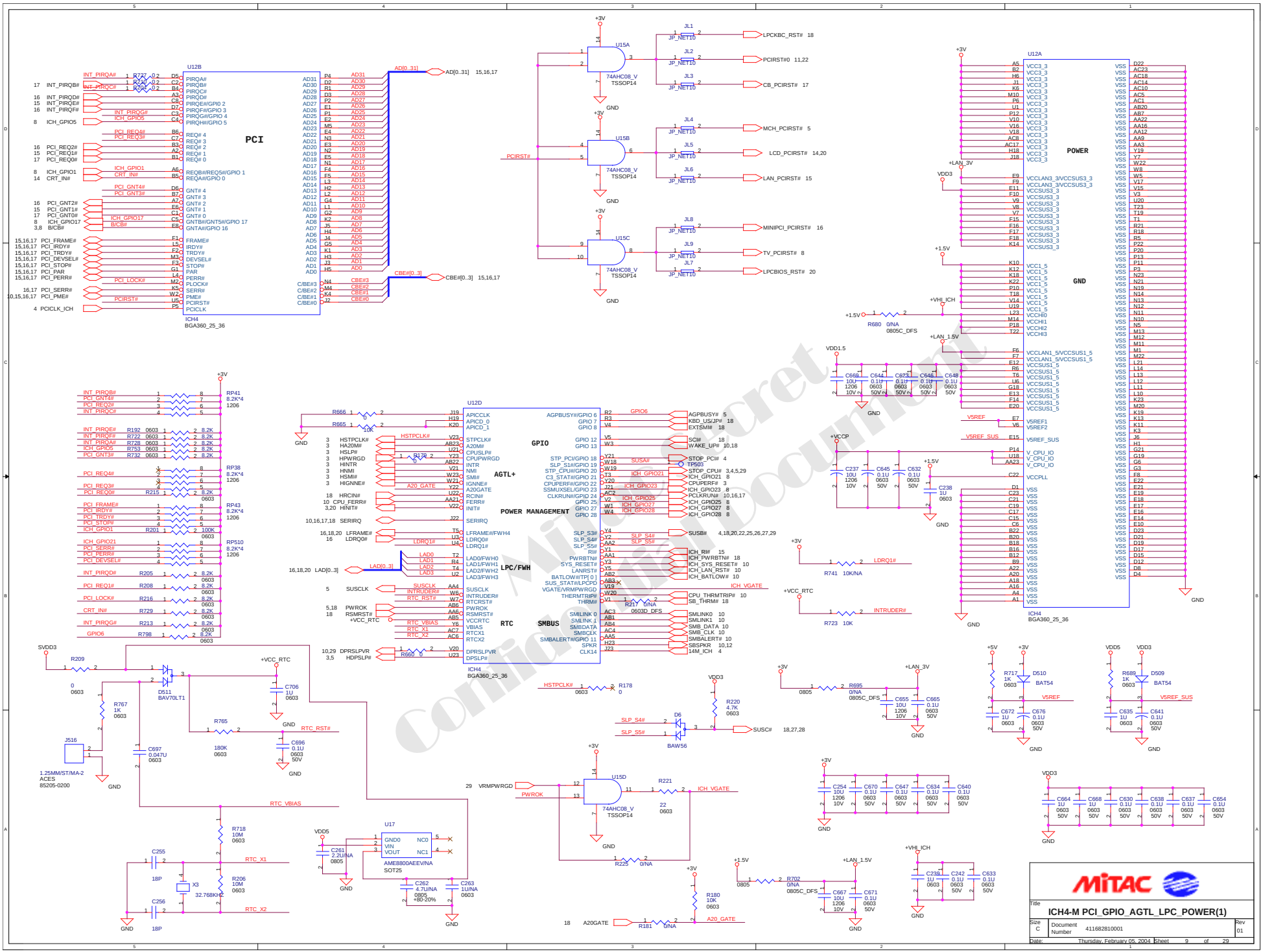

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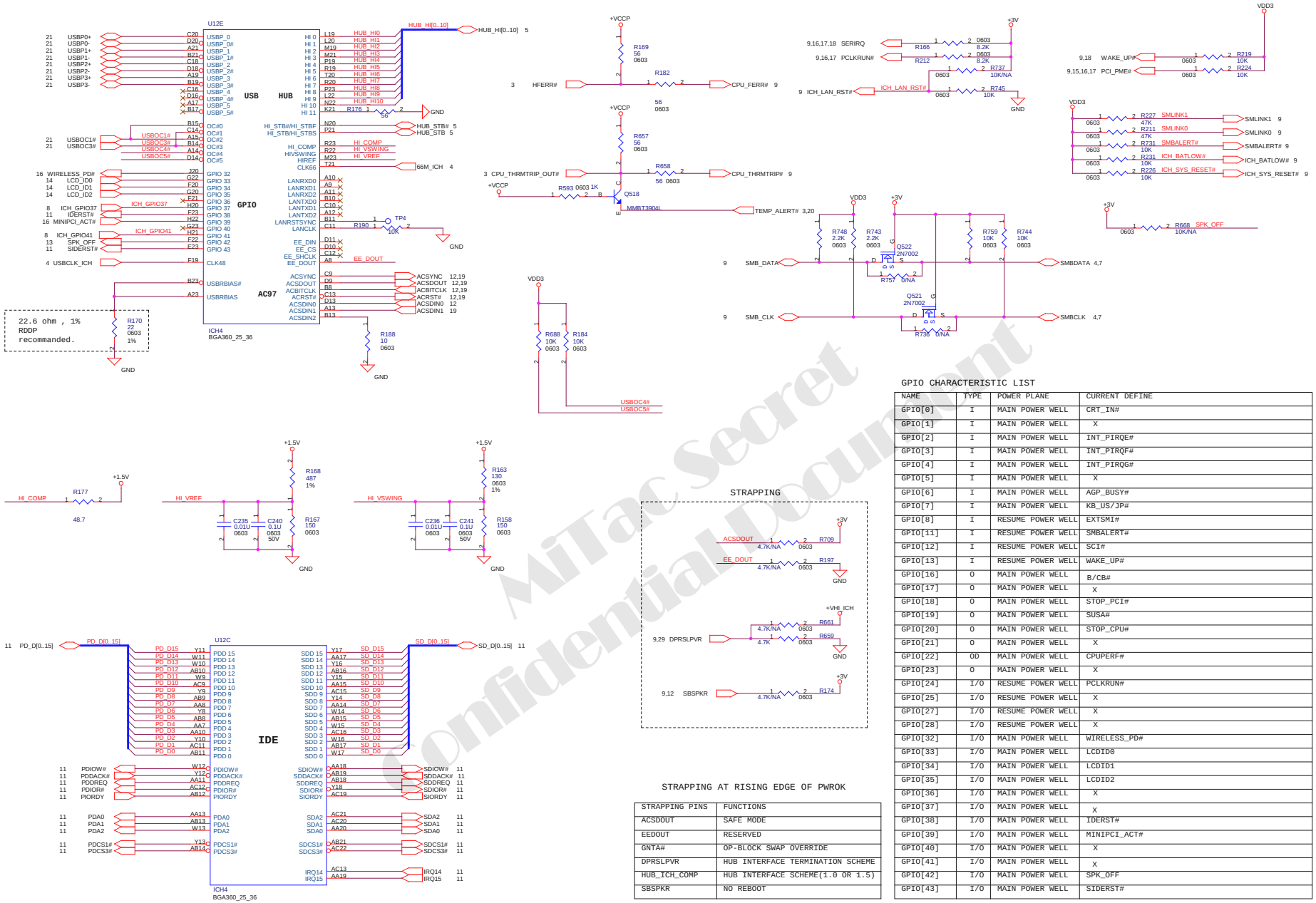

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GPIO CHARACTERISTIC LIST

NAME	TYPE	POWER PLANE	CURRENT DEFINE
GPIO[0]	I	MAIN POWER WELL	CRT_IN#
GPIO[1]	I	MAIN POWER WELL	X
GPIO[2]	I	MAIN POWER WELL	INT_PIRQE#
GPIO[3]	I	MAIN POWER WELL	INT_PIRQF#
GPIO[4]	I	MAIN POWER WELL	INT_PIRQG#
GPIO[5]	I	MAIN POWER WELL	X
GPIO[6]	I	MAIN POWER WELL	AGP_BUSY#
GPIO[7]	I	MAIN POWER WELL	KB_US/JP#
GPIO[8]	I	RESUME POWER WELL	EXTSMI#
GPIO[11]	I	RESUME POWER WELL	SMBALERT#
GPIO[12]	I	RESUME POWER WELL	SCI#
GPIO[13]	I	RESUME POWER WELL	WAKE_UP#
GPIO[16]	O	MAIN POWER WELL	B/CB#
GPIO[17]	O	MAIN POWER WELL	X
GPIO[18]	O	MAIN POWER WELL	STOP_PCI#
GPIO[19]	O	MAIN POWER WELL	SUSA#
GPIO[20]	O	MAIN POWER WELL	STOP_CPU#
GPIO[21]	O	MAIN POWER WELL	X
GPIO[22]	OD	MAIN POWER WELL	CPUPERF#
GPIO[23]	O	MAIN POWER WELL	X
GPIO[24]	I/O	RESUME POWER WELL	PCLKRUN#
GPIO[25]	I/O	RESUME POWER WELL	X
GPIO[27]	I/O	RESUME POWER WELL	X
GPIO[28]	I/O	RESUME POWER WELL	X
GPIO[32]	I/O	MAIN POWER WELL	WIRELESS_PD#
GPIO[33]	I/O	MAIN POWER WELL	LCDID0
GPIO[34]	I/O	MAIN POWER WELL	LCDID1
GPIO[35]	I/O	MAIN POWER WELL	LCDID2
GPIO[36]	I/O	MAIN POWER WELL	X
GPIO[37]	I/O	MAIN POWER WELL	X
GPIO[38]	I/O	MAIN POWER WELL	IDERST#
GPIO[39]	I/O	MAIN POWER WELL	MINIPCI_ACT#
GPIO[40]	I/O	MAIN POWER WELL	X
GPIO[41]	I/O	MAIN POWER WELL	X
GPIO[42]	I/O	MAIN POWER WELL	SPK_OFF
GPIO[43]	I/O	MAIN POWER WELL	SIDERST#

STRAPPING AT RISING EDGE OF PWROK

STRAPPING PINS	FUNCTIONS
ACSDOUT	SAFE MODE
EEDOUT	RESERVED
GNTA#	OP-BLOCK SWAP OVERRIDE
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME
HUB_ICH_COMP	HUB INTERFACE SCHEME(1.0 OR 1.5)
SBSPKR	NO REBOOT

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Title: ICH4-M USB_HUB_GPIO_AC97_IDE(2)

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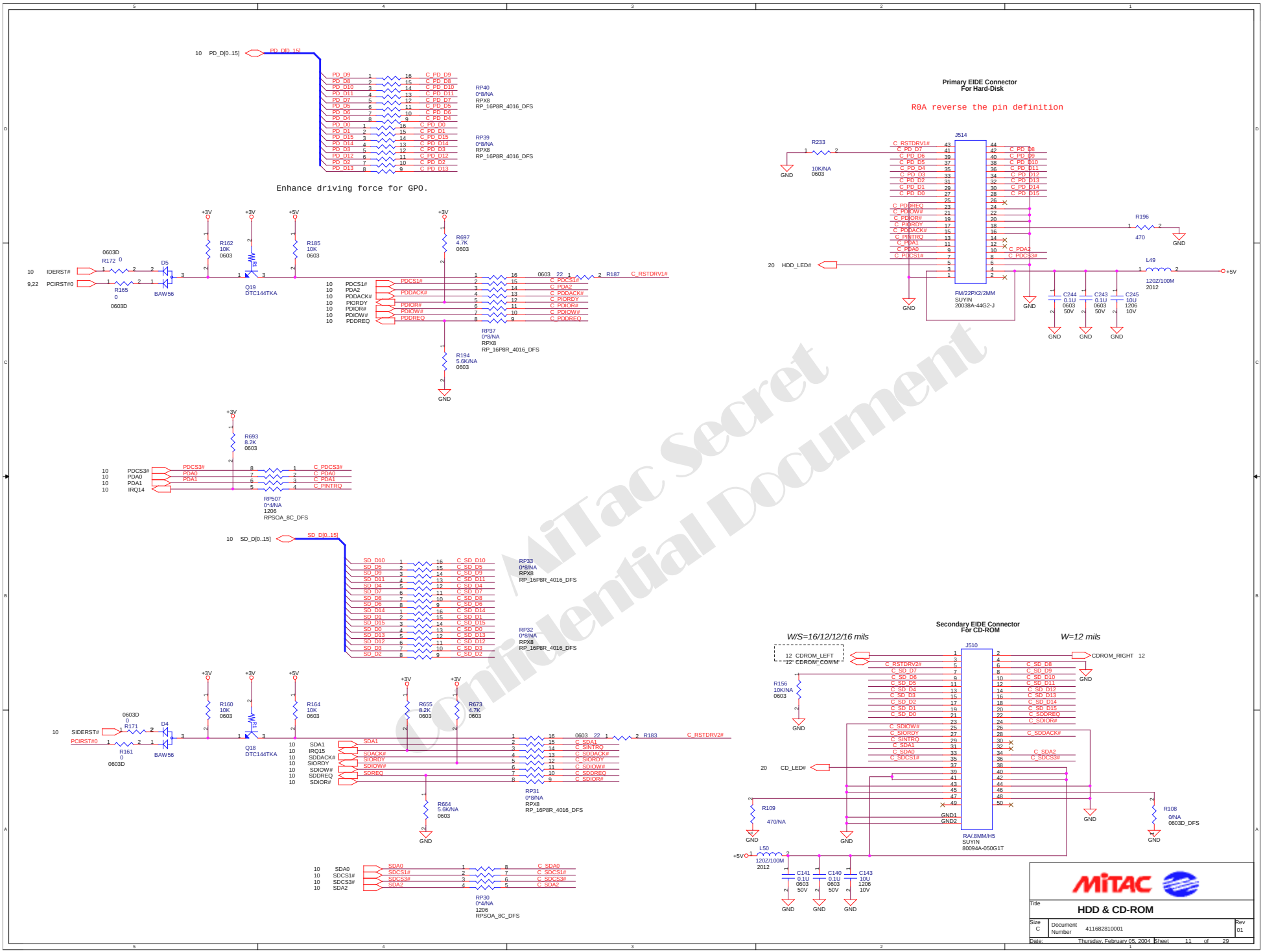

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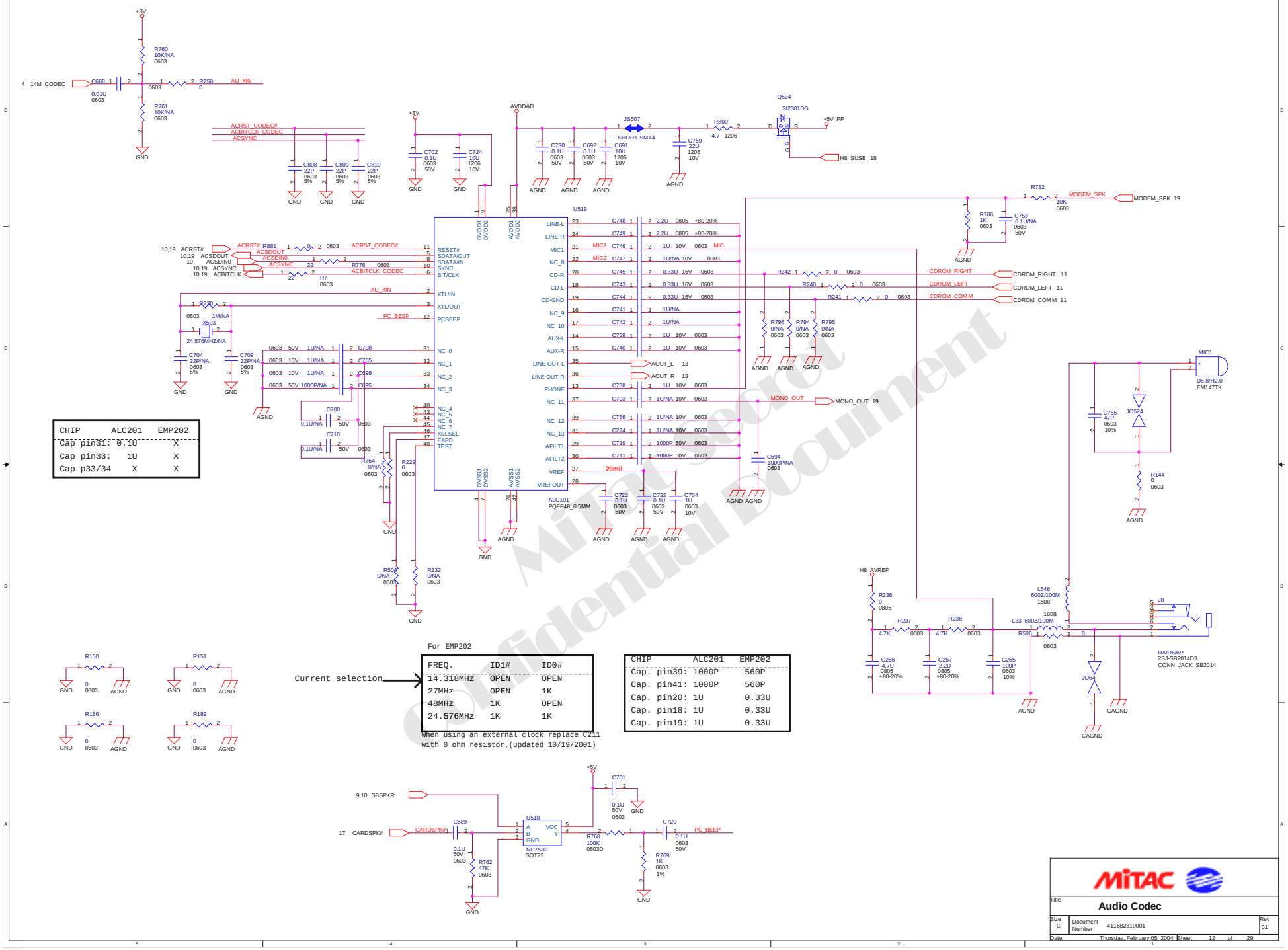

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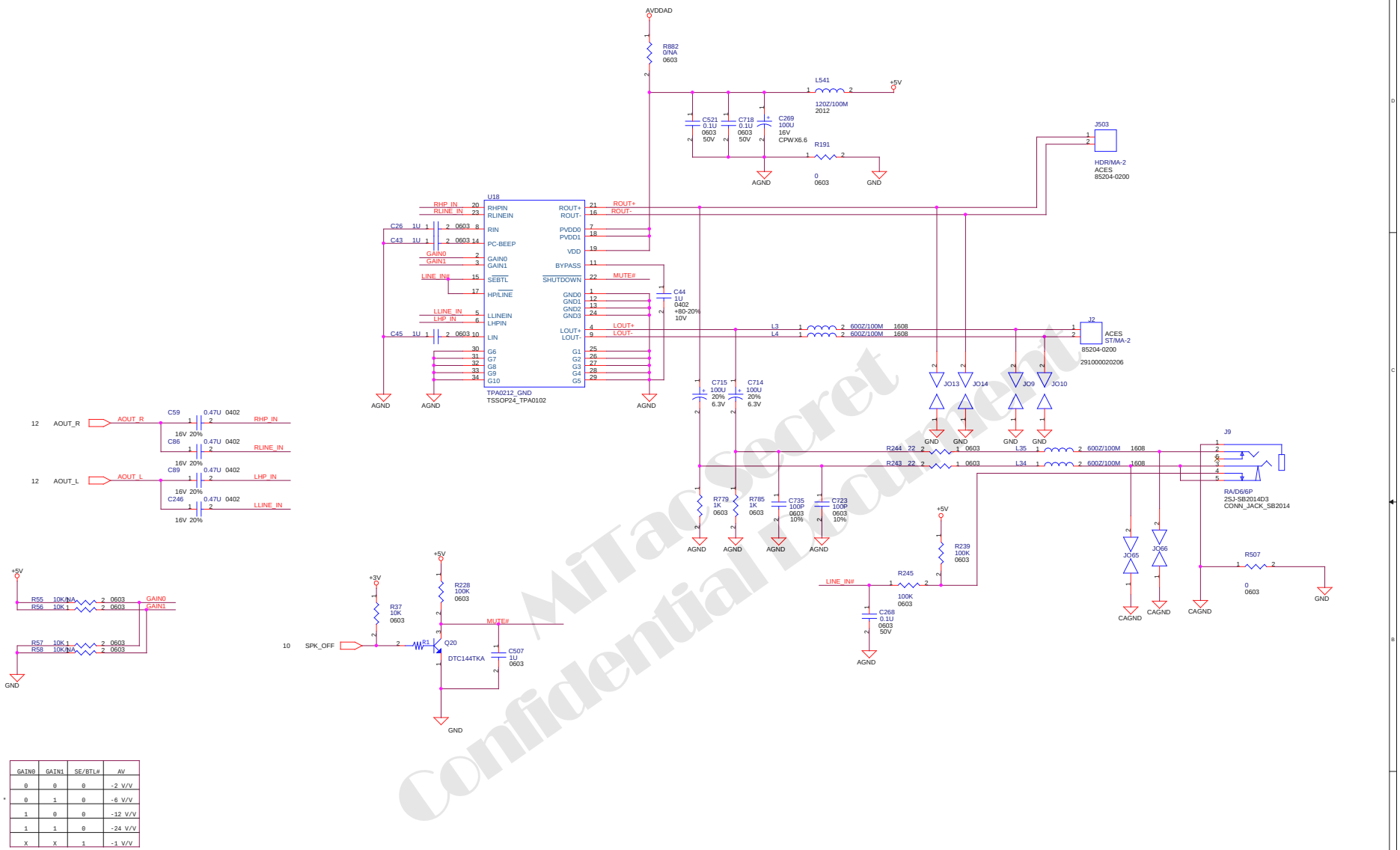

GAIN0	GAIN1	SE/BTL#	AV
0	0	0	-2 V/V
* 0	1	0	-6 V/V
1	0	0	-12 V/V
1	1	0	-24 V/V
X	X	1	-1 V/V

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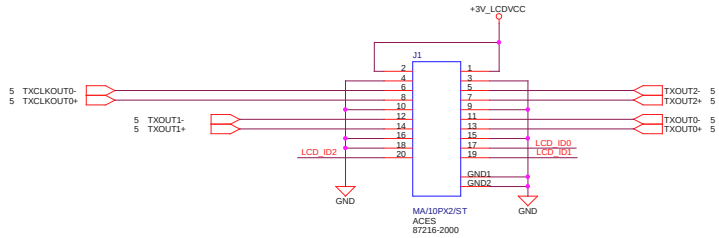
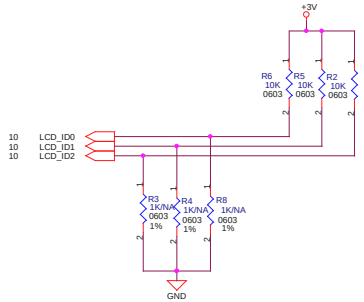
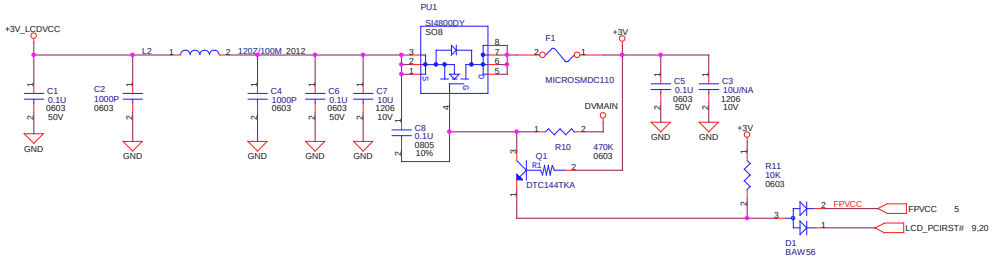
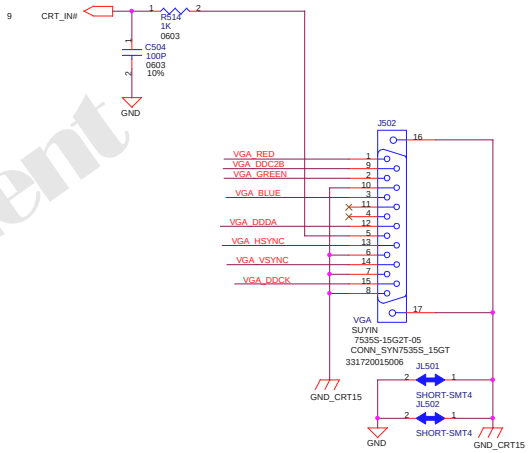
LCD CONNECTOR

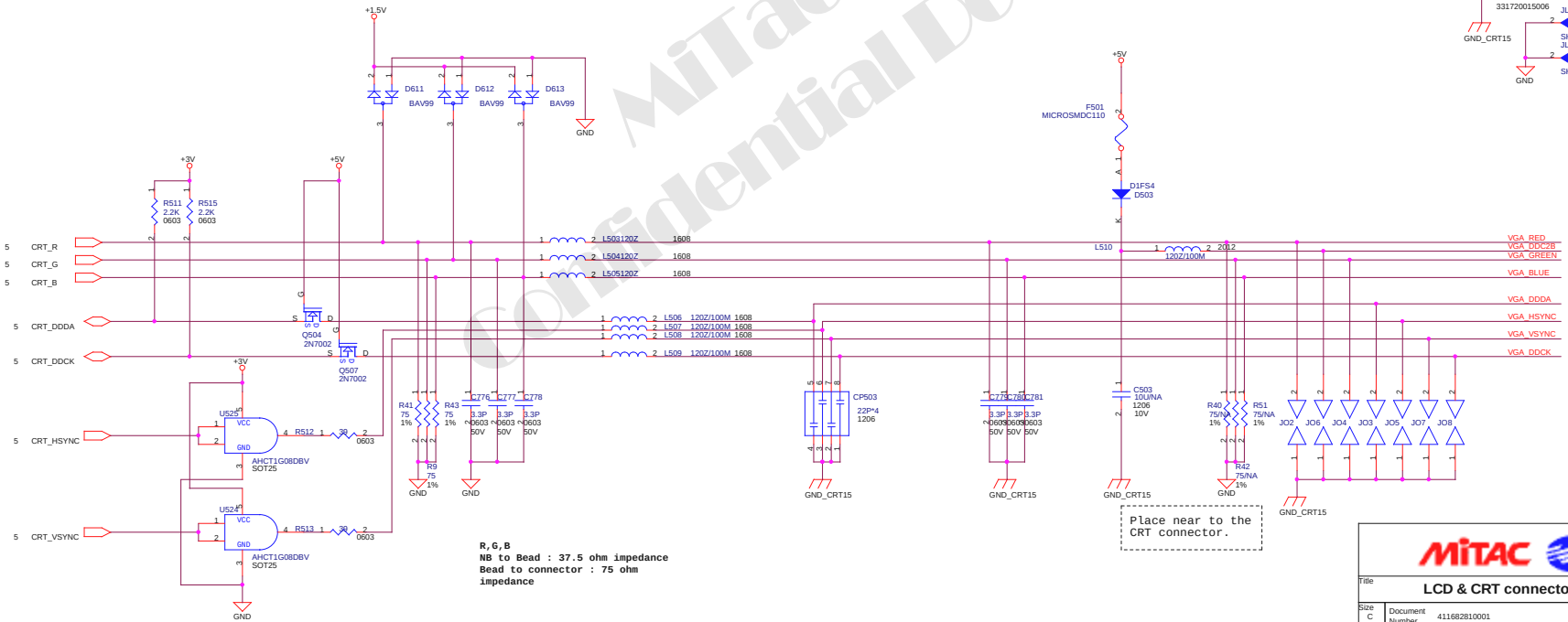
(1) AU 14" TFT XGA : B141XN04-2(UB141X03)
(2) Hydis 14" TFT XGA : HT14X13-102
(3) Chi-mei 14" TFT XGA : N141X6-L01
(4) Hydis 15" TFT XGA : HT15X34-100
(5) AU 15" TFT XGA : B150XG02
(6) Hannstar 15" TFT XGA : HSD150PX14-A
(7) Samsung 15" TFT XGA : LTN150XB-L03
(8) AU 15" TFT SXGA+ : B150PG01











R,G,B
NB to Bead : 37.5 ohm impedance
Bead to connector : 75 ohm impedance

Place near to the CRT connector.

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Title: LCD & CRT connector

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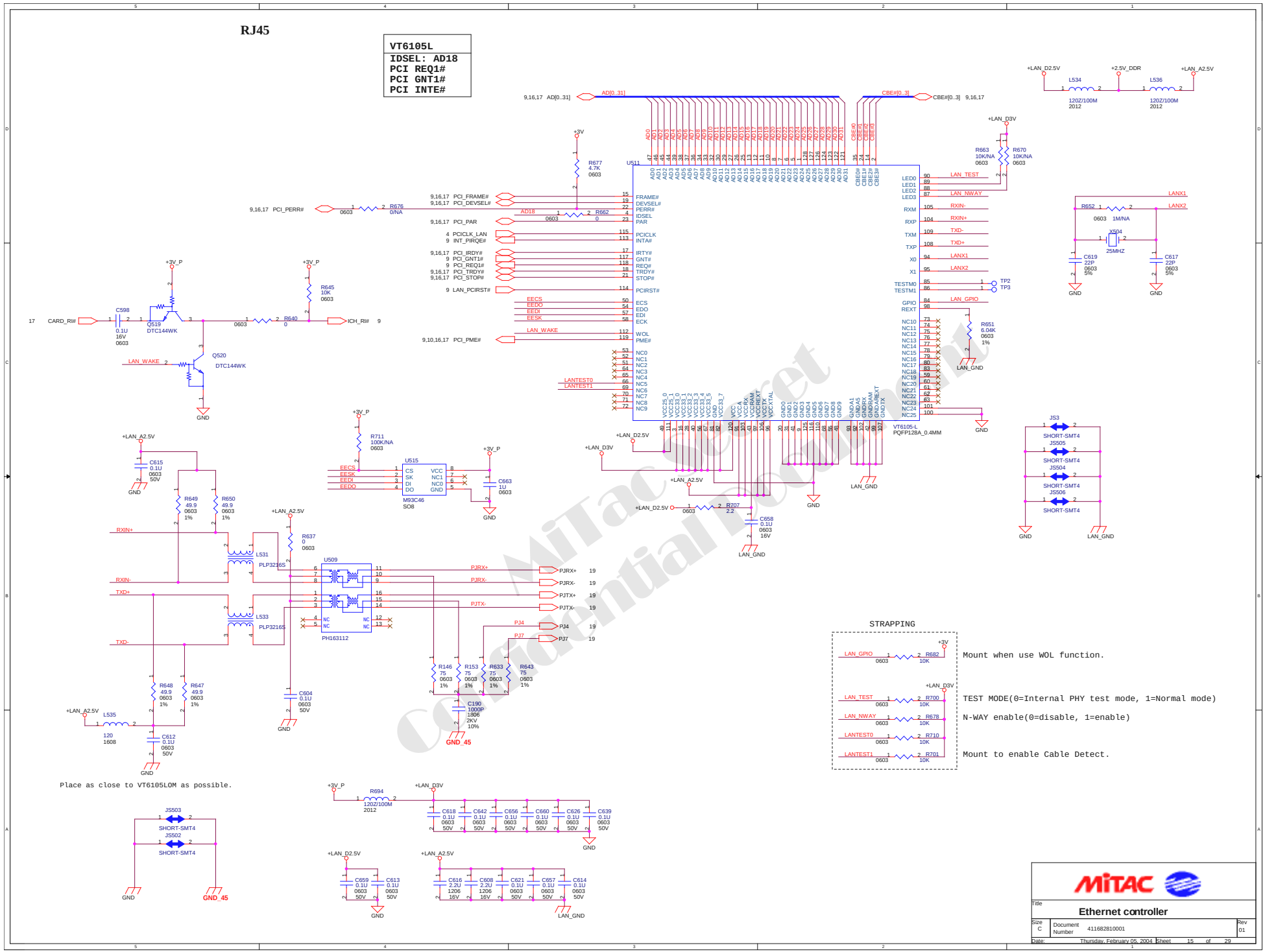

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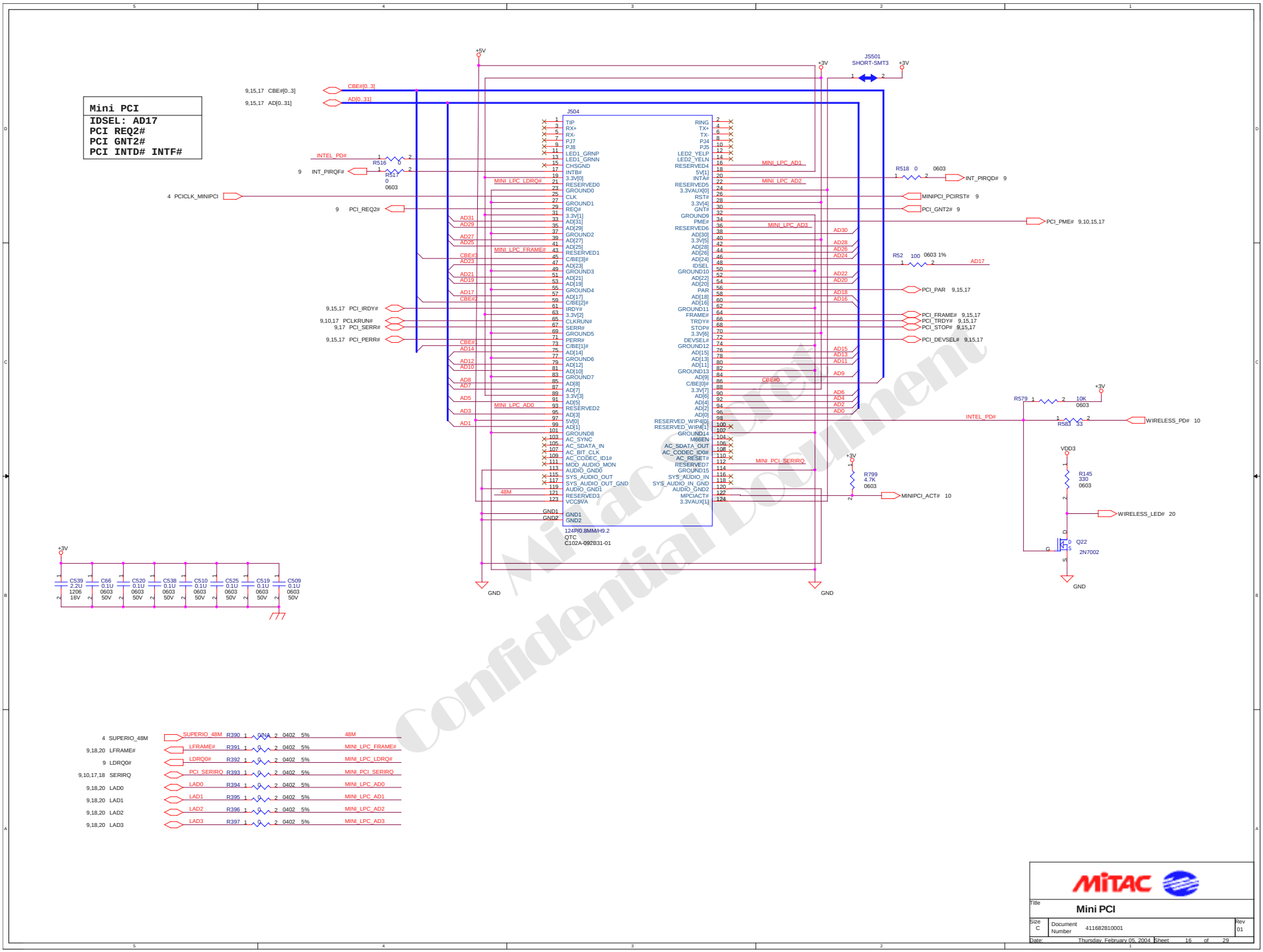

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CARDBUS CONTROLLER

SIGNAL	PC CARD PULL UP	SIGNAL	PC CARD PULL UP	SIGNAL	PC CARD PULL UP
CCD#1	+3V	CRST#	CARD_VCC	CPERR#	CARD_VCC
CCD#2	+3V	CSERR#	CARD_VCC	CINT#	CARD_VCC
CBLOCK#	CARD_VCC	CDEVSEL#	CARD_VCC	CIRDY#	CARD_VCC
CSTOP#	CARD_VCC	CTRDY#	CARD_VCC	CREQ#	CARD_VCC
		CVS1	+3V	CSTSCHG#	CARD_VCC
		CVS2	+3V	CAUDIO	CARD_VCC

PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE

PCI1410A
IDSEL : AD19
PCI REQ0#
PCI GNT0#
PCI INTB#

FOR 1410

U510 PCI1410 PQFP144_0.5MM

For 16 bit card

U513 TPS2211 SSOP16

ONLY FOR OZ6812

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Title: CardBus (PCI1410A)

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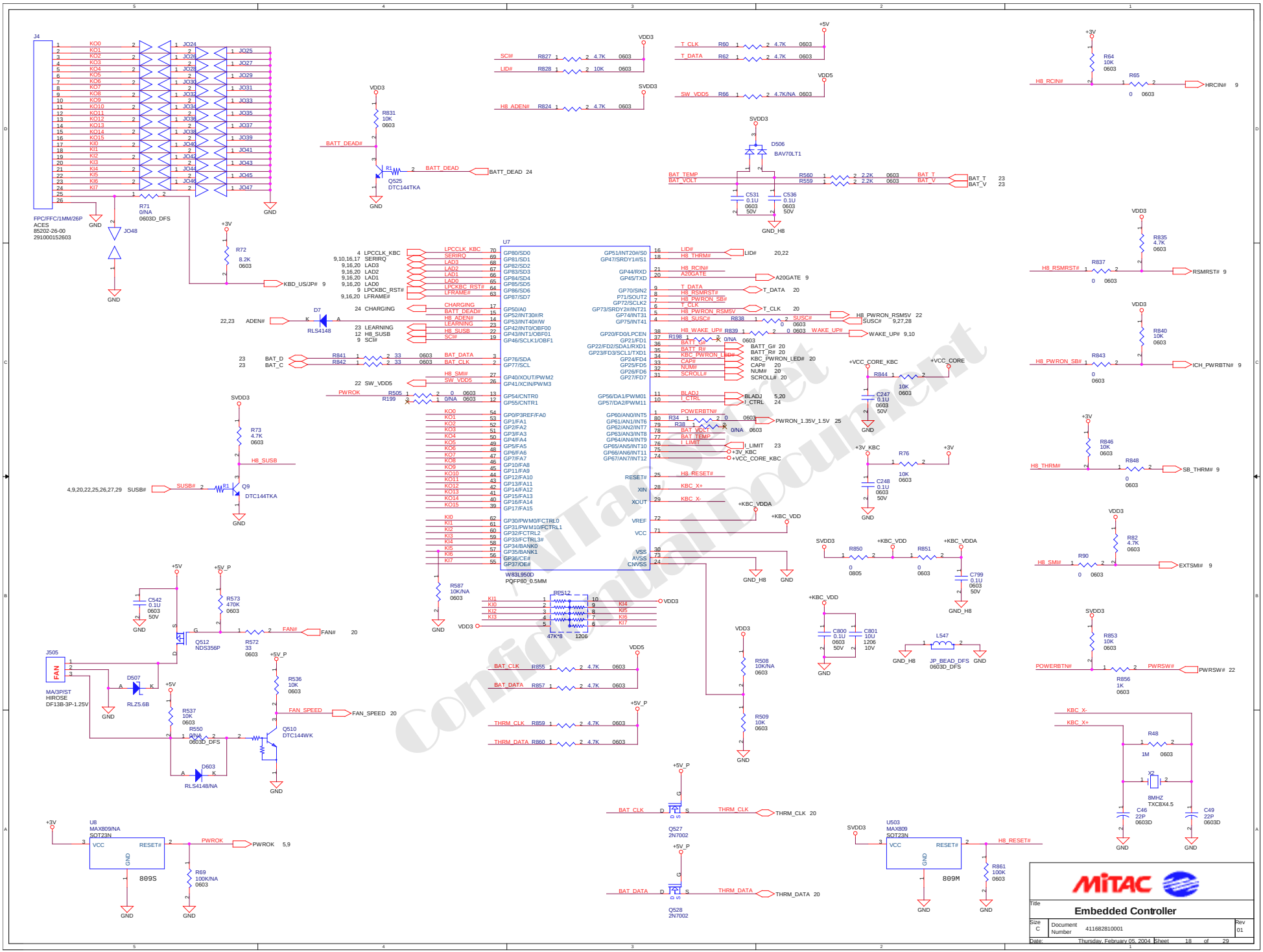

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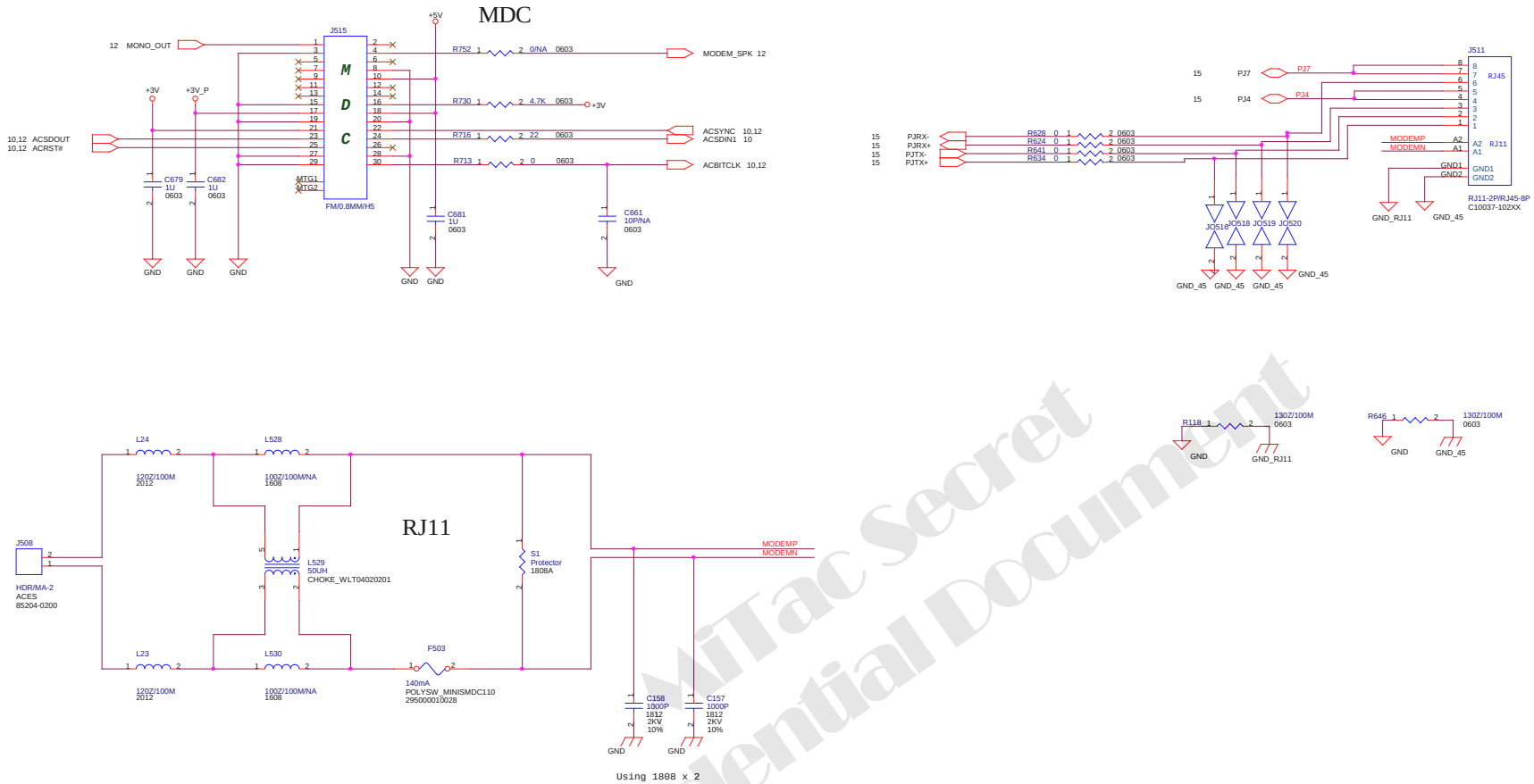

Using 1808 x 2

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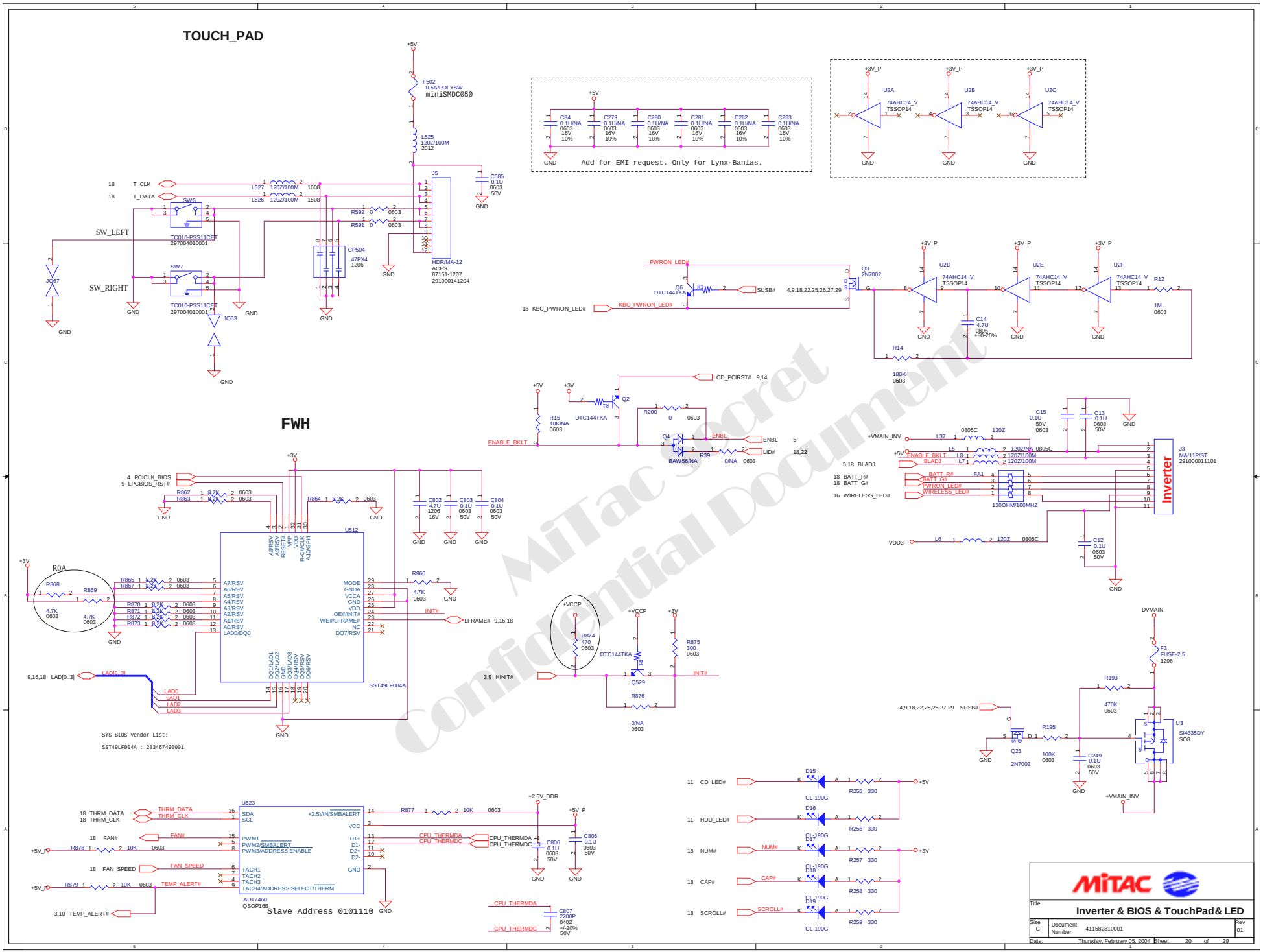

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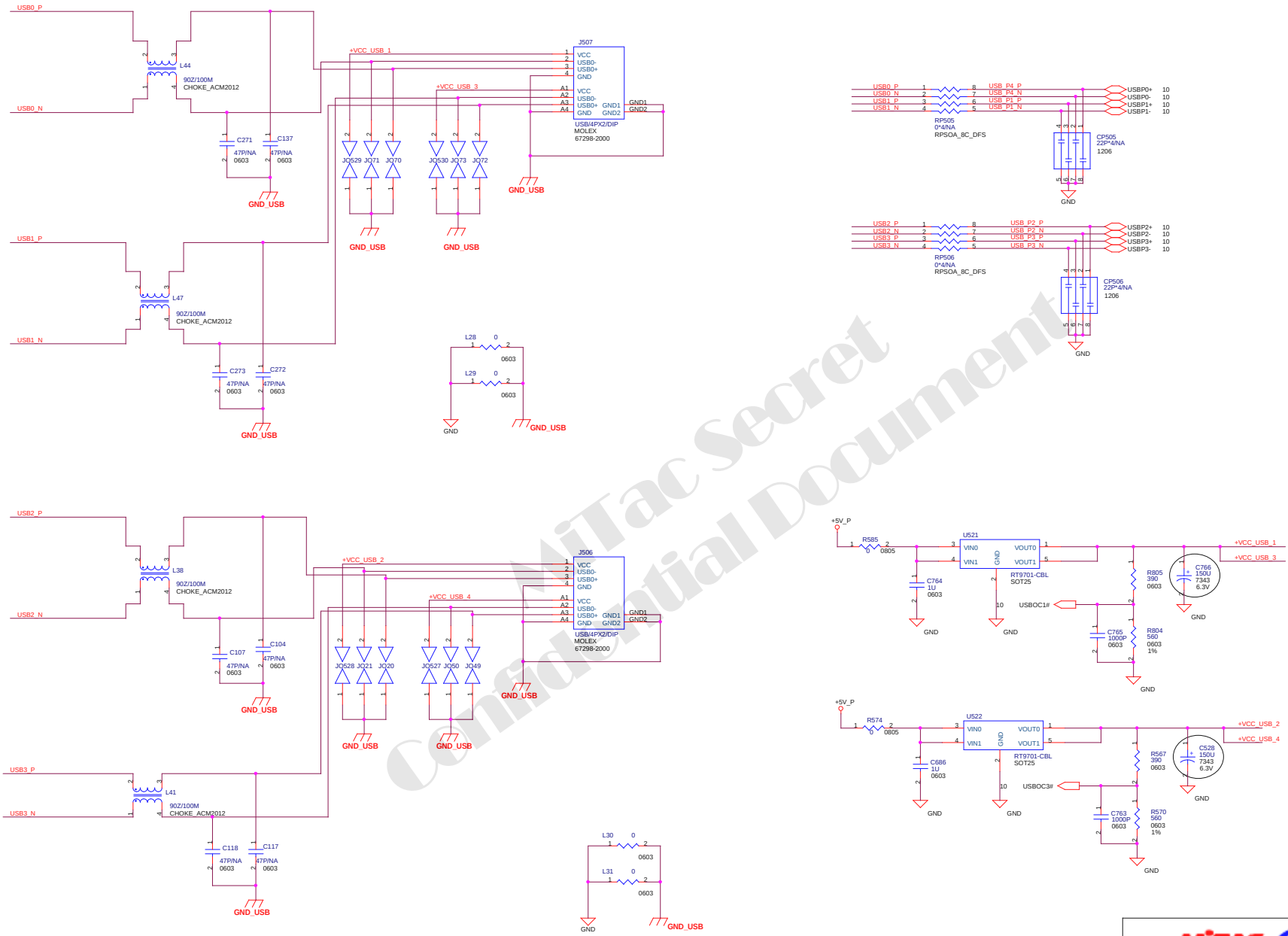

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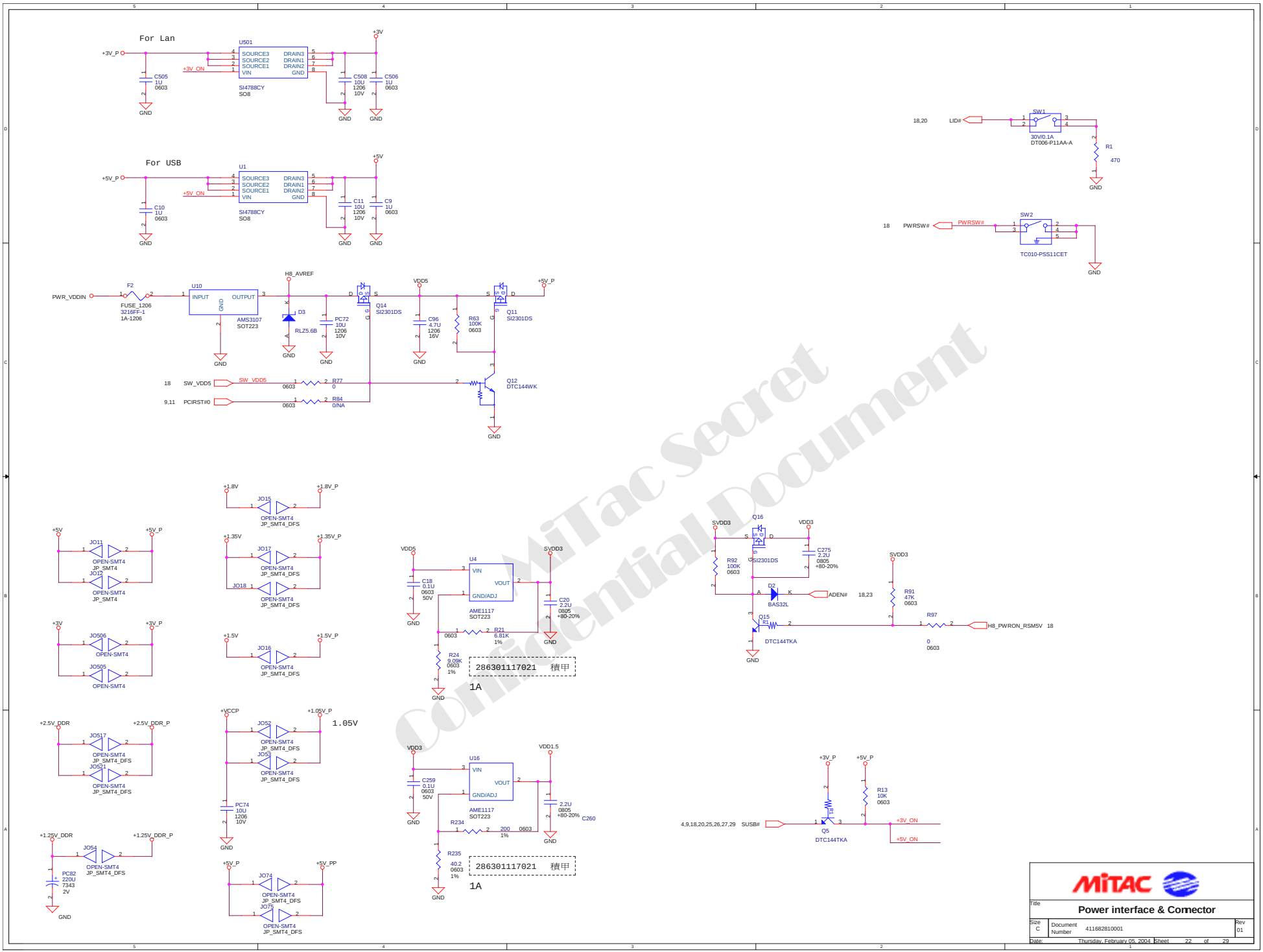

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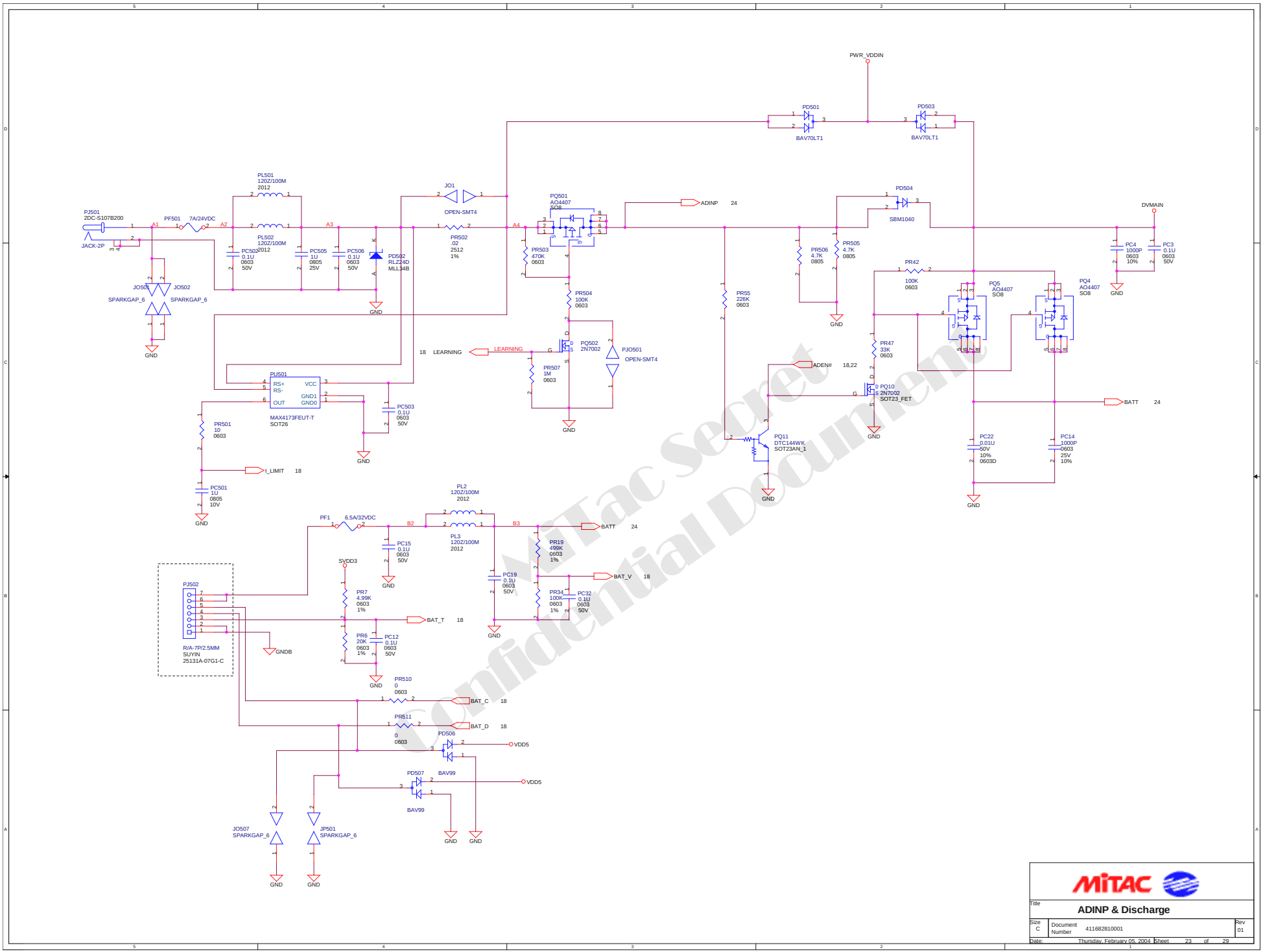

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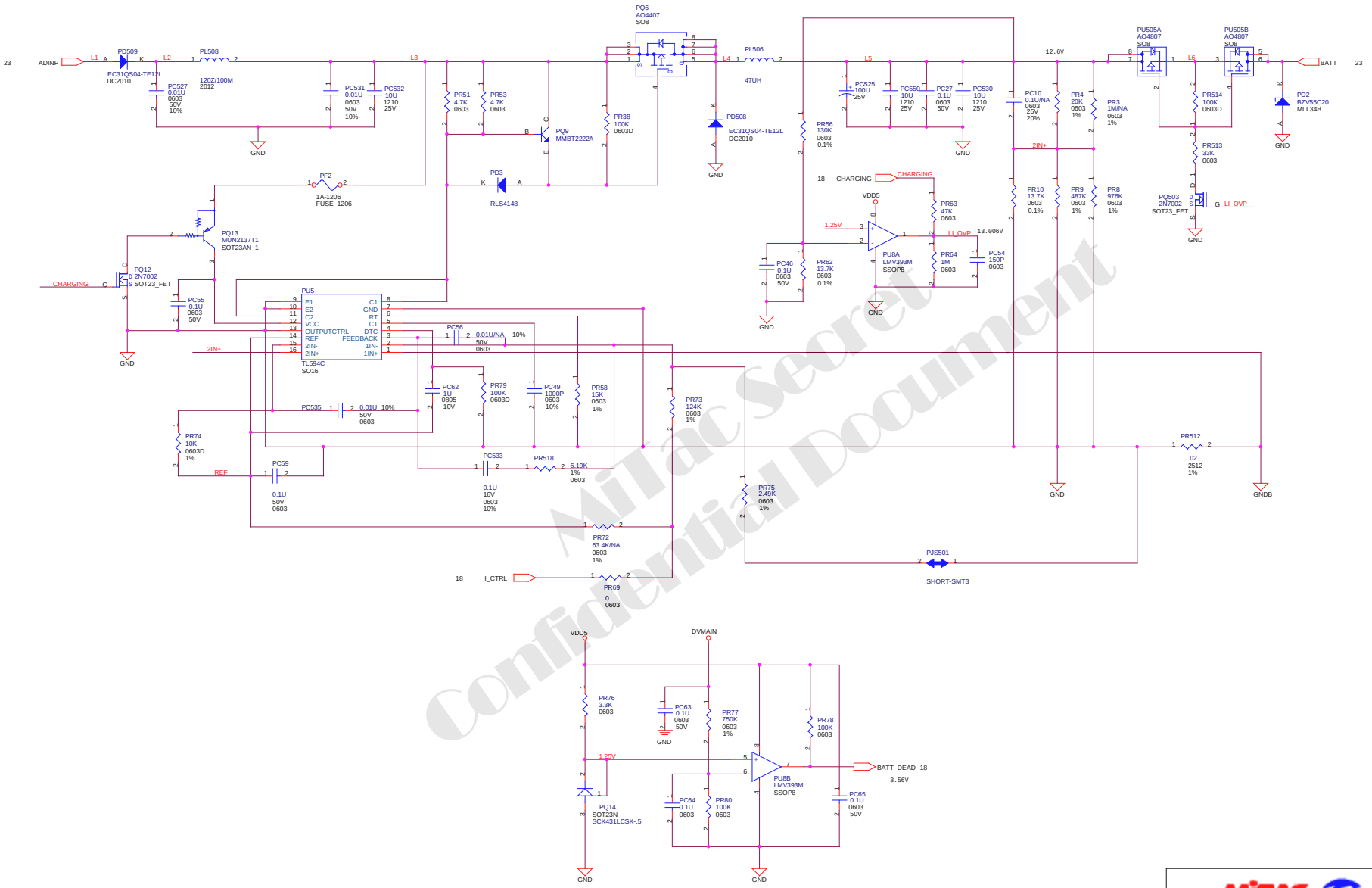
CHARGING



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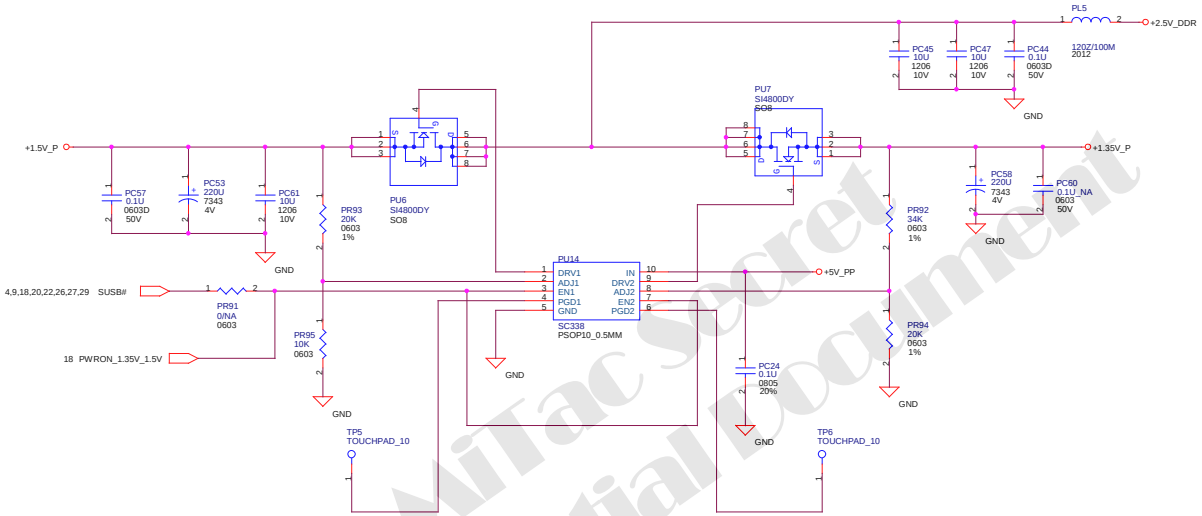

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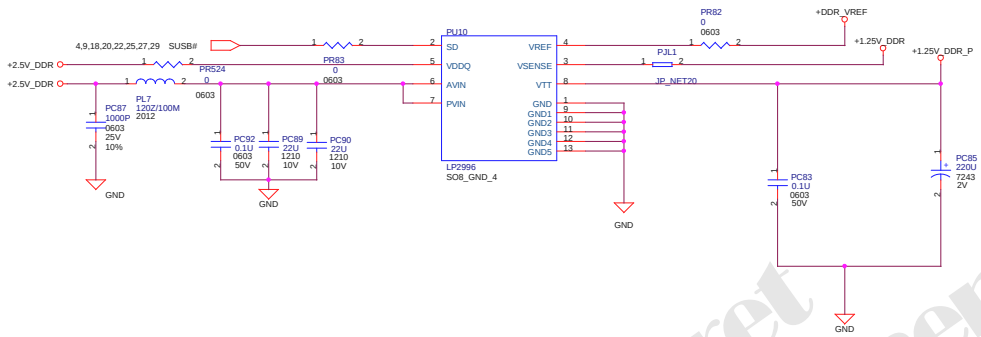

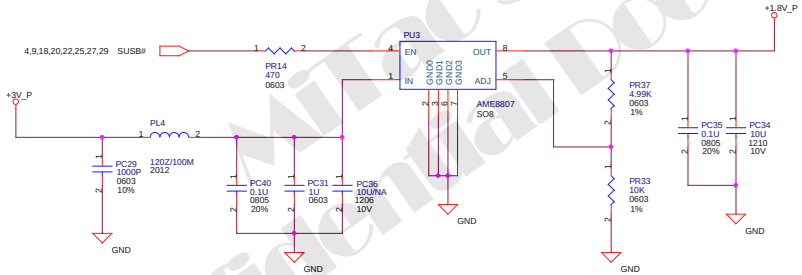

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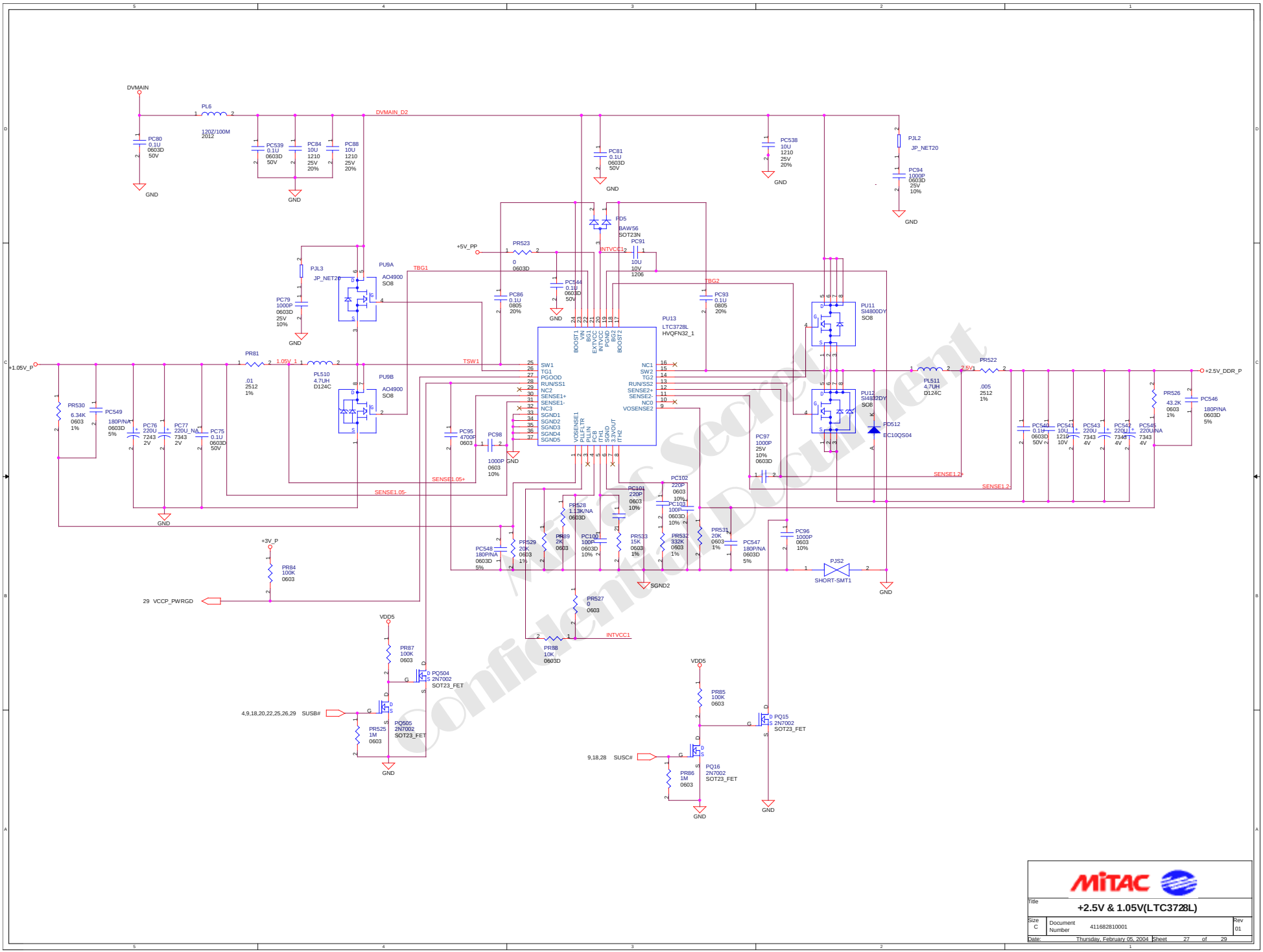

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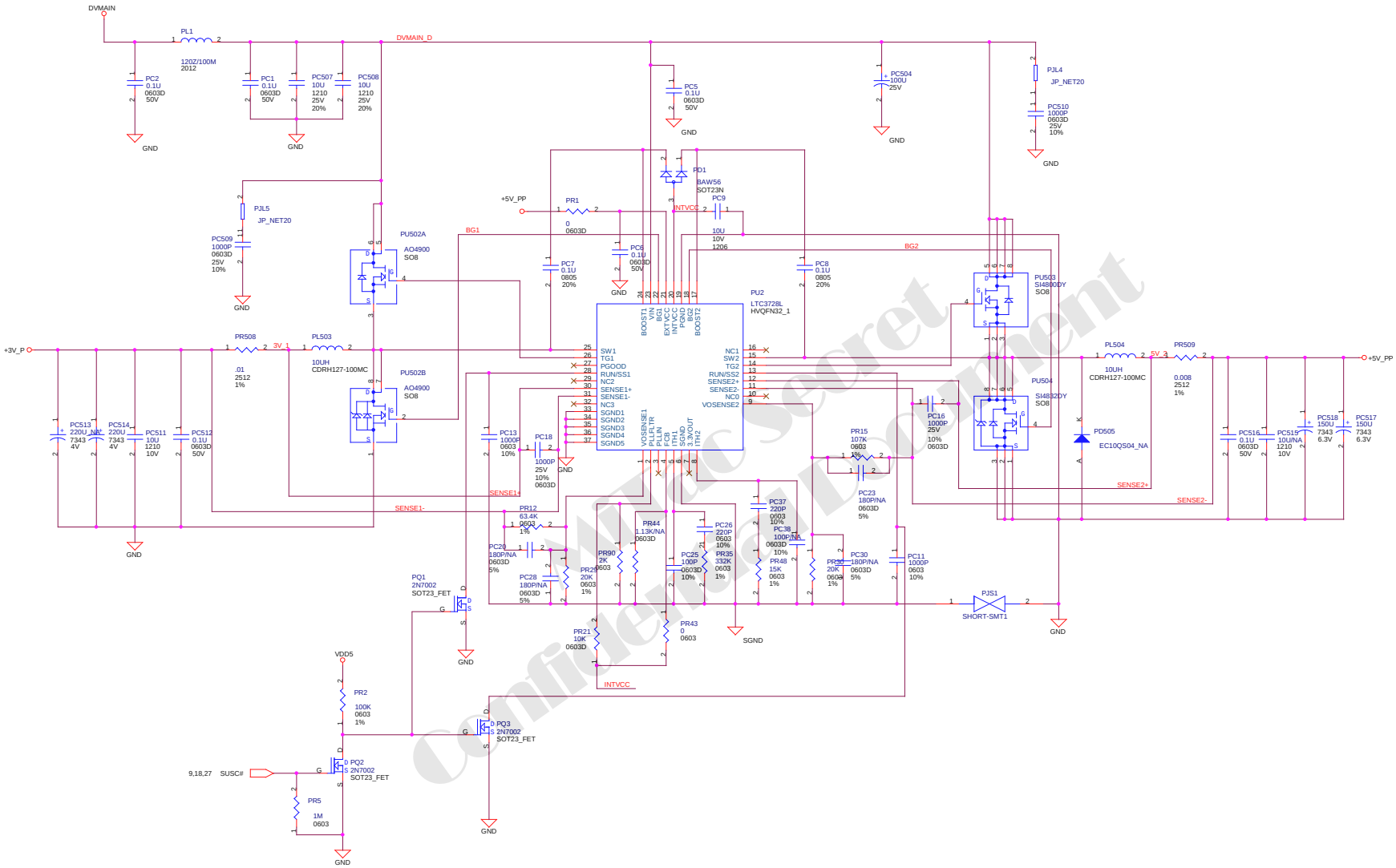

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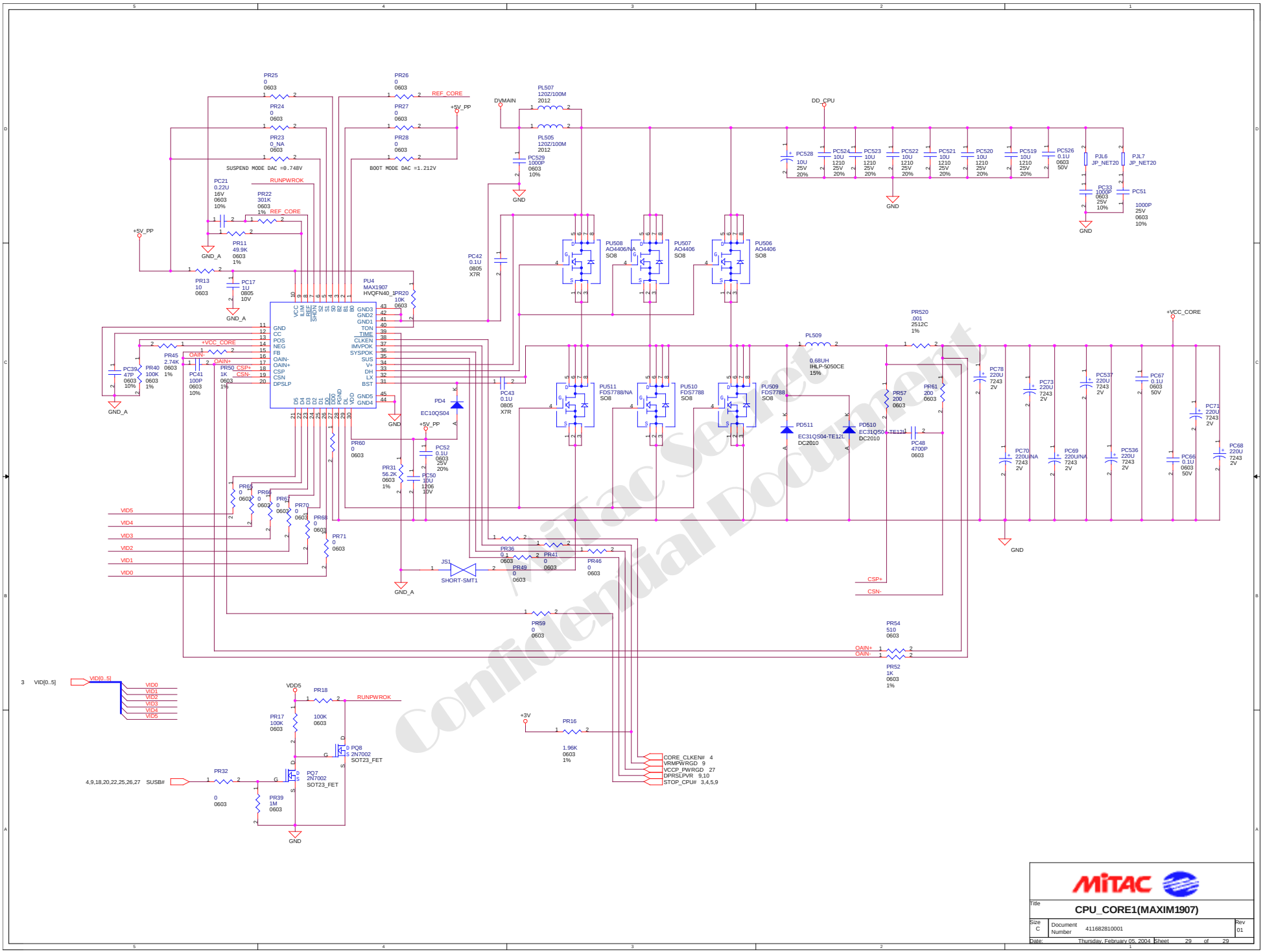

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Reference Material

INTEL Banais Processor	INTEL, INC.
Intel Montara-GME GMCH	Intel, INC.
Intel 82801DBM ICH4-M	Intel, INC.
WINBOND W83L950D Universal Controller	WINBOND, LTD.
PhaseLink PLL207-151	PhaseLink,INC
VIA Rhine III VT6105LOM	VIA, INC
System Explode View	Technology Corp / MiTAC
8089P Hardware Specification	Technology Corp / MiTAC

SERVICE MANUAL FOR 8089P

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